SP-12
SAMPLING PERCUSSION SYSTEM
SERVICE MANUAL

By Steve Davies

Version 1.1

INTRODUCTION

The SP-12 is a powerful and complex instrument. E-mu Systems Inc. intends this manual to be an aid to the experienced service technician only.

To service the SP-12 you should know about the 7400 series of digital logic, the Z-80 CPU and its family of peripherals, ADCs and DACs, op-amps, transistors and power supplies. The minimum equipment required to service and repair the SP-12 are, a digital multimeter, a 60Mhz dual trace oscilloscope and basic technician hand tools.

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We feel obliged to remind you that any modification of an SP-12 other than as specified by a factory authorized Engineering Change Order (ECO) will void the warranty of the instrument.

Please read this manual thoroughly before attempting to service the SP-12. If you feel unsure about working on the instrument, contact our service department.

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SECTION 1

OVERVIEW

This section briefly covers the functions of the SP-12. It is not meant to replace the Owners Manual, however all functions will be covered. We will relate front panel functions to specific hardware wherever possible to aid in understanding the machine. The SP-12 is relatively easy to use and most functions will display messages to help you along.

Let's begin with a front panel overview. (see fig. 1) The panel is divided up into 7 modules. Each module has a specific group of functions. The Performance Module has all the real time controls, such as the play buttons and the sequencer RUN/STOP and RECORD. The sliders have multiple functions as selected by the TUNE/DECAY, MIX, MULTIMODE button. The play buttons are assignable by pressing SELECT. TAP/REPEAT is used to enter a desired tempo by tapping the button or repeat a sound being played automatically.

The Master Control Module has a 16 character by 2 line backlit LCD display which the CPU uses to communicate with the user. For data entry there is a numeric keypad and ENTER button. The TEMPO button is used to change the current tempo value. Right and left arrow buttons increment or decrement the value above the flashing cursor. YES and NO buttons let you make decisions and the mix and metronome ouput levels are set here.

To the left of the master control is the Programming Module. The creation of songs and segments is the function of this module. In Segment Mode selection of auto correct, time signature, segment length and metronome rate are controlled here. Step programming and segment copy as well as swing functions are controlled by Segment Mode. Song Mode is used for creating songs by linking segments together. Mix and tempo changes are programmed here.

Above and to the left is the Set-Up Module. It has the controls for all of the multi modes such as multi pitch and multi level. It also has channel assigment for routing sounds to different channels and loop/truncate for modifying sounds that have been sampled. Deleting sampled sounds as well as changing their decay are initiated using this module. MIDI parameters are selected and the special function menu is controlled here. The mix is defined and selected using this module. The special function section contains all the functions not on the front panel and any that have been added as software updates.

To the right of Set-Up is the Cassette/Disk Module. All disk and tape read, write, verify and catalog functions are initiated using this module.

Next is the Sync Module. This is used for selecting the method of clocking the sequencer. The options are: internal sync where the internal sequencer clock is the master. MIDI, where the MIDI clock triggers the sequence. SMPTE, which uses a SMPTE track from a film or video source and clock, which uses a sync track on tape, another drum machine or sync box.

Last we have the Sample Module. This allows the user to sample up to 32 of his (or her) own sounds. The standard machine has 1.2 seconds of sample memory that can be expanded to 5 seconds. The sound can then be truncated, looped, decayed or pitch shifted and assigned to any output channel.

PROGRAMMING OVERVIEW

The SP-12 has two main programming modes, Segment and Song. Segments are drum patterns that vary in length from 1 to 99 measures. The user creates segments that contain the song's introduction, main groove, fills and the ending. The segments are then linked together using song mode to create the song.

PERFORMANCE CONTROLS

All the sounds are accessed through this module. Only eight sounds at a time can be played. Which eight are played can be changed by using the select button. It is possible to "rip off" a sound by playing two sounds at the same time when they are assigned to the same output channel. The software assigns the last sound played as the priority. This can be used to good effect on the hi-hat to simulate the foot opening and closing it. This can also cause problems if you try to play two sounds at the same time on the same channel.

The buttons are dynamic but not polyphonic. This means that if two buttons are played at the same time both sounds will be as loud as the hardest hit button. The dynamic buttons work by sensing the vibration of the PCB with a piezo crystal. This voltage is read by the ADC and used to set the sounds output level.

The TAP/REPEAT button is used for entering a tempo or repeating a sound. The button is tapped several times to enter the desired tempo. The CPU reads the rate of tapping to determine the new tempo value. This works whenever the display's flashing cursor is under the current tempo value.

Repeat is used for automatically repeating a sound. This is done by holding the repeat button down and pressing the desired sound. It will repeat at the auto correct rate, i.e. if auto correct is 16th notes the sound will occur every 16th note.

The RUN/STOP button is used for starting and stopping the sequencer. There is also a footswitch input for this function.

The RECORD button is used for both segment and song recording. To use in segment mode press and hold it then press the RUN/STOP button. Sounds can now be played and the sequencer will record them. The segment is like a tape loop, after the last beat is played, it will wrap around and begin again. If the machine is in song mode, pressing record enters record immediately. Segment numbers, mix and tempo changes can now be entered and a song created.

The TUNE/DECAY, MIX and MULTIMODE buttons select the function of the sliders. The display shows graphically what effect the sliders will have on the sound. When new sounds are assigned to the play buttons, the sliders will now effect the new sounds.

MASTER CONTROL MODULE

This module is used for communicating with the operating software. The LCD display will ask the user for data or decisions regarding the current module he (or she) is using and display any pertinent information. The display has 16 characters by 2 lines and can display low resolution graphics. Just about every button on the front panel will write a new message to the display. For example if the TUNE/DECAY, MIX, MULTIMODE button is pressed the display will show bar graphs of the current TUNE/DECAY value. The sliders can now be moved to change the value while it is being graphically displayed.

The display is backlit by an electroluminescent panel. This allows using it in subdued lighting.

Pressing the tempo button will only change the position of the flashing cursor. The cursor position indicates what value will change using the keypad, arrow buttons or slider. All data is input using a slider, keying in the number or changing a current value with the arrow keys. After a value is changed or entered, enter is pressed to tell the CPU to save the new value.

The mix out pot controls the mix out level only. It does not effect the channel outputs. The metronome pot controls the volume of the metronome in the mix out only.

SET-UP MODULE

This module is used for many different features. All the multimodes are turned on and off in this module. Multipitch is used to assign a sound to all the play buttons with each button a different pitch. The pitch of each button can be changed with the sliders. Multipitch assigns a different level to every button using the same sound. The sliders also control the level of each individual button's sound.

The dynamic buttons are turned on and off using Set-up 14.

Mixes for songs are defined using Set-up 15. This is used in conjunction with the sliders in mix mode to set the sound levels.

Channel assignment is programmable using set up 17. Each sound can be assigned to any of the eight output channels. The eight channels have different amounts of filtering.

DECAY/TUNE is selected using Set-up 18. A sound can be tuned or decayed but not both. The sliders are used to change the decay or tuning of the sounds while the display shows what the value is.

All sounds can be looped or truncated using Set-up 19. This applies only to sampled sounds. The display shows the loop and truncation points.

Any single user sound can be deleted using Set-up 20

The first step of a song can be changed using Set-up 21. This is useful for starting a song in the middle to listen to a recent change.

MIDI parameters are selected using Set-up 22. Options are omni and poly, and pitch keys on or off.

Special is used for special functions and adding features through software updates. Press Set-up 23 and use slider A to scroll through the functions.

CASSETTE/DISK MODULE

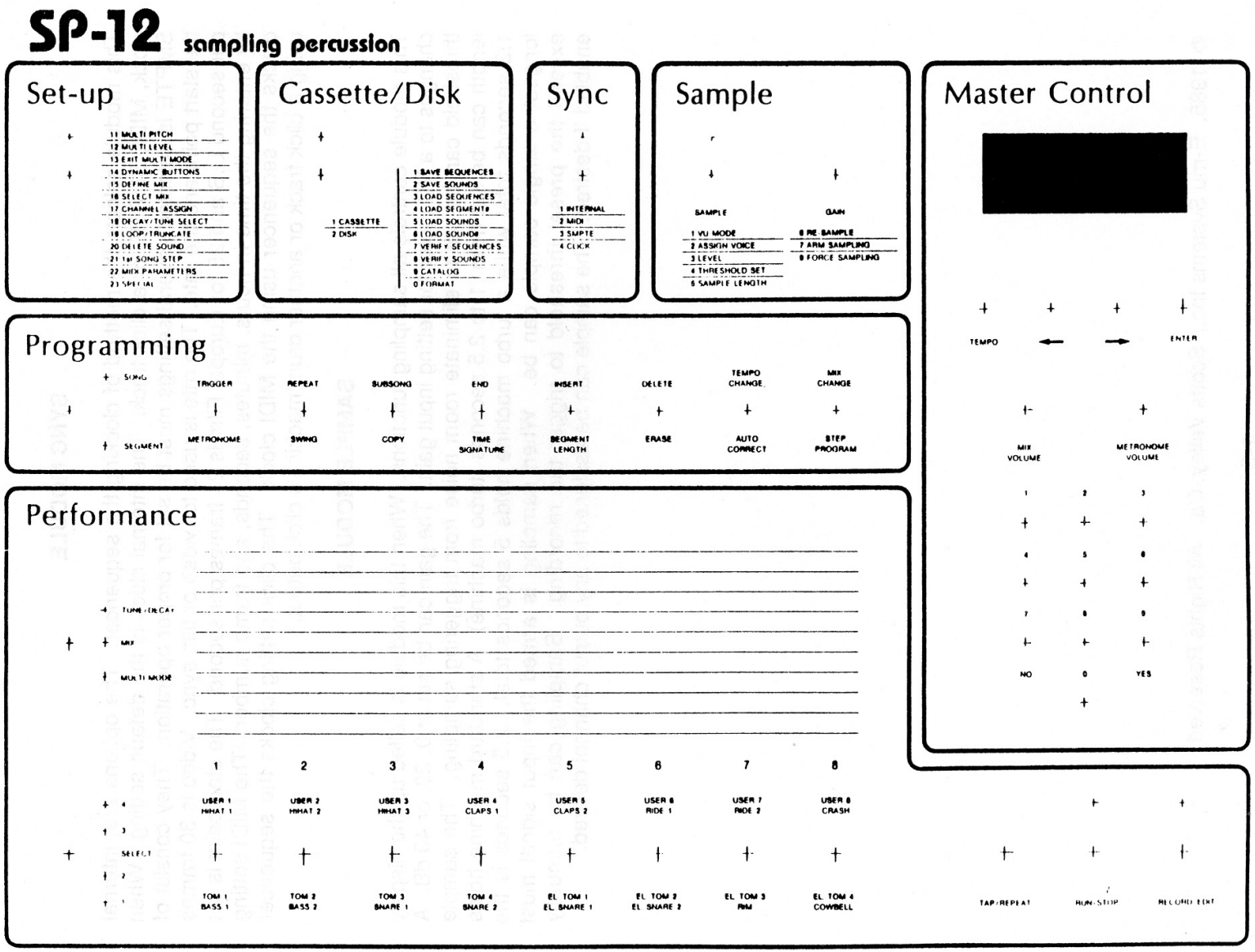
This module is used to save sequencer programs and sound data. A regular audio cassette or the Commodore disk drive can be used. Separate sounds or segments can be saved or retrieved as well as the entire memory. The disk format function is used to format blank discs. Verify is used to check the data was correctly saved on the disc or tape.

SYNC MODULE

This module selects the method of clocking the sequencer. The options are: internal clock, MIDI, SMPTE, or a click track. The internal clock is the default setting. When SMPTE is selected several settings must be set for proper operation. They consist of the start point and the rate. The rate is used for video or film sync. Video is 30 frames per second U.S and 25 for Europe. Film is 24 frames per second. The start point is set by entering the time in hours, minutes, seconds, and frame number. The MIDI setting clocks the sequencer using the MIDI clock. The click setting clocks the sequencer using a click track or another drum machine's click output.

SAMPLE MODULE

This module controls all sampling functions. When this module is called up the display changes to a VU meter for setting input gain. The gain can be set at 0, 20, or 40 dB. A threshold can be set to eliminate room noise from triggering sampling. The sample length can be set from .1 to 2.5 seconds (turbo machine) A standard machine holds 1.2 seconds total while a turbo machine holds 5 seconds total. 2.5 seconds is the longest a single sample can be. When sampling is armed the input signal must exceed the preset threshold to trigger the recording. Sampling can be manually enabled if desired. The sample can be assigned to any output channel desired.


SP-12 sampling percussion
Set-up
11 MULTI PITCH
12 MULTI LEVEL
13 EXIT MULTI MODE
14 DYNAMIC BUTTONS
15 DEFINE MIX
16 SELECT MIX
17 CHANNEL ASSIGN
18 DECAY/TUNE SELECT
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20 DELETE SOUND
21 1st SONG STEP
22 MIDI PARAMETERS
23 SPECIAL
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2 DISK
1 SAVE SEQUENCES
2 SAVE SOUNDS
3 LOAD SEQUENCES
4 LOAD SEGMENTS
5 LOAD SOUNDS
6 LOAD SOUNDS
7 VERIFY SEQUENCES
8 VERIFY SOUNDS
9 CATALOG
0 FORMAT
Sync
1 INTERNAL
2 MIDI
3 SMPTE
4 CLICK
Sample
SAMPLE
1 VU MODE
2 ASSIGN VOICE
3 LEVEL
4 THRESHOLD SET
5 SAMPLE LENGTH
GAIN
6 RE-SAMPLE
7 ARM SAMPLING
8 FORCE SAMPLING
Master Control
TEMPO
ENTER
MIX VOLUME
METRONOME VOLUME
NO
YES
Programming
SONG
SEGMENT
TRIGGER
METRONOME
REPEAT
SWING
SUBSONG
COPY
END
TIME SIGNATURE
INSERT
SEGMENT LENGTH
DELETE
ERASE
TEMPO CHANGE
AUTO CORRECT
MIX CHANGE
STEP PROGRAM
Performance
TUNE/DECAY
MIX
MULTI MODE
SELECT
1
2
3
4
5
6
7
8
USER 1 HIHAT 1
USER 2 HIHAT 2
USER 3 HIHAT 3
USER 4 CLAPS 1
USER 5 CLAPS 2
USER 6 RIDE 1
USER 7 RIDE 2
USER 8 CRASH
TOM 1 BASS 1
TOM 2 BASS 2
TOM 3 SNARE 1
TOM 4 SNARE 2
EL TOM 1 EL SNARE 1
EL TOM 2 EL SNARE 2
EL TOM 3 RIM
EL TOM 4 COWBELL
TAP/REPEAT
RUN/STOP
RECORD/EDIT
E-mu Systems, Inc.

Fig. 1
1-6

SECTION 2

INTERFACE SPECIFICATION

THE MIDI INTERFACE
(Musical Instrument Digital Interface)

MIDI is a serial 5 milliamp current loop interface between two or more computer controlled musical instruments. It uses optoisolators and non grounded inputs to prevent ground loops. It runs at a 31.25 kBaud rate and does not use any handshaking. Each MIDI connection requires two wires to complete the loop. The hardware used is very simple. The output is an open collector driver, typically a 7407, and a series resistor. The return line is a series resistor which is connected to 5 volts. The input is an LED used in the standard 6N138 optocoupler. (see schematic page 2 of 21) MIDI uses standard 5 pin DIN connectors for input, output and thru signals.

THE SMPTE INTERFACE
(Society of Motion Picture and Television Engineers)

To understand SMPTE a very basic knowledge of video is extremely helpful. If you do not understand video, we suggest finding a book or two on the subject and checking it out. SMPTE time code is used primarily for editing video tape. It is recorded on a spare audio track and has a 80 bit code that uniquely identifies each frame. The format looks like this:

| Hours | Minutes | Seconds | Frame # |

SMPTE has other uses such as syncing 2 24 track tape machines together or film to sound syncing. It is also used in studios as the master sync track and for autolocators on multitrack tape machines. Since SMPTE records the absolute value, it is superior to click tracks and regular sync tones. The SP-12 sequencer can be programmed to start at 1 hour 20 minutes 30 seconds 21st frame and it will start precisely at that moment. If the master tape is fast forwarded, the SP-12's sequencer will fast forward until sync is achieved then begin playing. There are two SMPTE transmission rates we use. For video in the U.S.A 2400 baud is used. This number is derived from 30 frames per second times 80 bits per frame. For most of the rest of the world 2000 baud is used. This corresponds to 25 frames a second times 80 bits. Film uses 24 frames per second and gets by using 2000 baud. The SMPTE input needs to see at least 250 millivolts to read the time code reliably. For more information on how we generate and read SMPTE see Section 3, the Theory of Operation.

SYNC

This input is for sync tracks that have been recorded on tape. The standard is 24 pulses per quarter note. The signal can also originate from other drum machines or sequencers. Inputs other then 24 pulses can be accomodated by changing the click input divisor. The range is 02 to 99. The click input needs to see a signal amplitude of at least 4 volts and a pulse width of 1 ms.

CASSETTE

The cassette interface uses the SMPTE circuitry to generate and read data on a standard audio cassette. The data encoding format is different from SMPTE to accomodate sound and sequencer information. The cassette input needs at least 250 millivolts of signal to work reliably. The rate of data transfer is 2400 baud.

DISK

The disk interface is designed to work with the Commodore disk drive. The interface conforms to the Commodore serial bus standard. Basically the SP-12 is programmed to act like a Commodore 64 and store files on the disk as the Commodore would. The interface uses the standard Commodore disk drive cable. The connector is a 6 pin DIN type with the following pin out:

PIN	DESCRIPTION
1	serial service request in
2	ground
3	serial attention in/out
4	serial clock in/out
5	serial data in/out

For more information on this interface see the CPU Theory of Operation or the Commodore 64 Programmers Reference Guide.

SECTION 3

SP-12 THEORY OF OPERATION

OVERVIEW

The SP-12 is very much like the Drumulator in that is uses multiplexed audio controlled by a custom designed microcontroller and uses a Z-80 CPU. There are some major differences like the 12 bit data format and user sampling. Knowledge of the Drumulator will be helpful in learning how the SP-12 functions.

The simplified block diagram (see fig. 2) shows the entire SP-12. Starting from the top left we see that the sliders are read by an ADC circuit. The value is read from the data bus by the Z-80 when it selects the ADC chip.

The LEDs are treated as a write only port. They are connected to a latch which the Z-80 writes to when an LED needs to be turned on or off.

The display is connected to the data bus and treated as a read/write port. All information for the user is written to this port in ASCII except for a few graphic symbols.

The pots are regular analog controls. The mix out pot is connected in the feedback loop of the mix out buffer amp. The metronome pot is connected from the metronome output to ground. The wiper is then summed into the mix out with the rest of the output channels. The sample gain pot has one end grounded and the other connected to the sample input jack. The wiper of the pot feeds the input buffer amp.

The buttons are set up in a matrix and decoded to determine which button was pushed. Two I/O ports are used for this. The first port is the decoder which the Z-80 writes to for row selection. The second port is used to read all the columns to determine which switch was pressed on the decoded row.

The Z-80 is the main CPU that runs the machine. It reads the buttons and sliders and writes to the display. It communciates with the world through the SIO (Serial Input Output). The instructions that run the machine are contained in two EPROMS. There is also static RAM for program variables, the CPU's stack and sequencer memory.

The CTC is used primarily for generating timed interrupts. The CPU is interrupted by the CTC to scan the buttons every 1.2 milliseconds. It also is used for sequencer timing and SMPTE/SYNC input and output timing.The microcontroller handles all the sound output control. It generates the memory timing and control signals as well as the

SP-12 Block Diagram

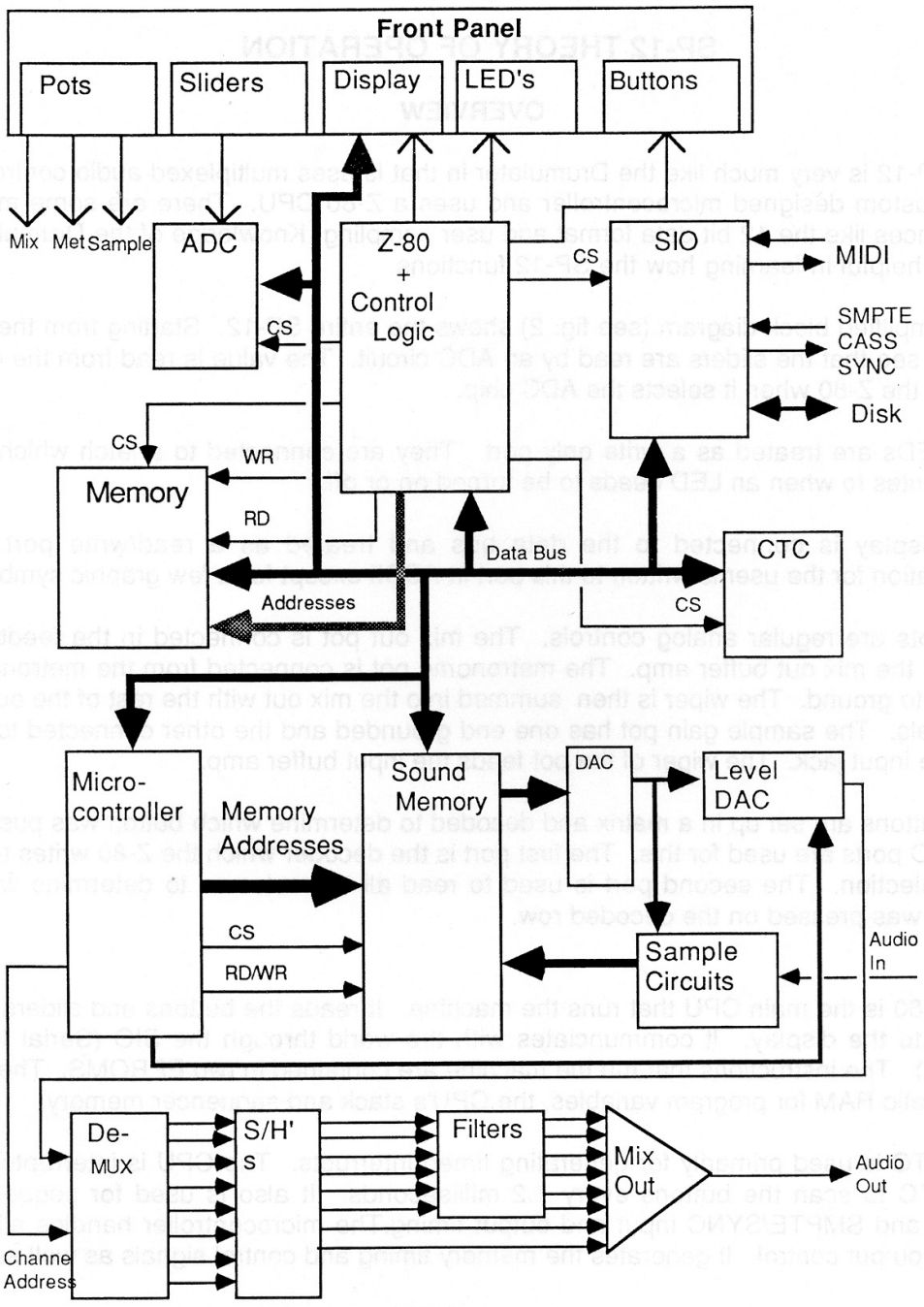

FIG 2

memory addresses. It also generates the signals for the sound level control registers and timing for the de-multiplexing of sounds.

The sound memory is a combination of EPROM and RAM. The standard sounds are stored in the EPROMS and any user sampled sounds are stored in the RAM. The RAM can be expanded from the standard 1.2 seconds to 5 seconds. This requires the installation of 18 8kX8 CMOS low power static RAMs and a PAL (Programmable Array of Logic) change. The sound RAM is powered by a lithium battery when the main power is shut off.

The DAC is a standard 12 bit linear device. It is used for playing and sampling sounds.

For signal level control a standard 8 bit multiplying DAC is used. The level value is stored in a register in the microcontroller. It is sent to the level DAC at the appropriate time to control the level of each sound separately.

The sample circuit uses the 12 bit sound DAC and a successive approximation register to digitize the incoming signal. This is done under CPU control.

The de-multiplexer separates the 8 channels then routes them to the sample/holds. Two channels (7+8) are direct outs. The rest of the channels are filtered. The channels are summed together at the mix out amp. There are 8 separate outputs independent from the mix out not shown on this diagram.

THE CPU AND FRONT PANEL

(see fig. 3)

The SP-12 uses a Z-80A processor running at 3.3 Mhz. Its memory consists of 24K Bytes of EPROM program memory and 40K Bytes of battery backed RAM. (16K standard, 24K optional) A 74HCT138 is used to decode the CPU's memory.

**********NOTICE**********

The SP-12 was designed to use 74HCT series logic instead of 74LS. We did this to lower the power requirements and use a smaller power supply. We do NOT recommend using 74LS chips as replacements for HCT as they overtax the power supply. There are a few locations where LS is used because of circuit loading, however the majority of TTL ICs are HCT.

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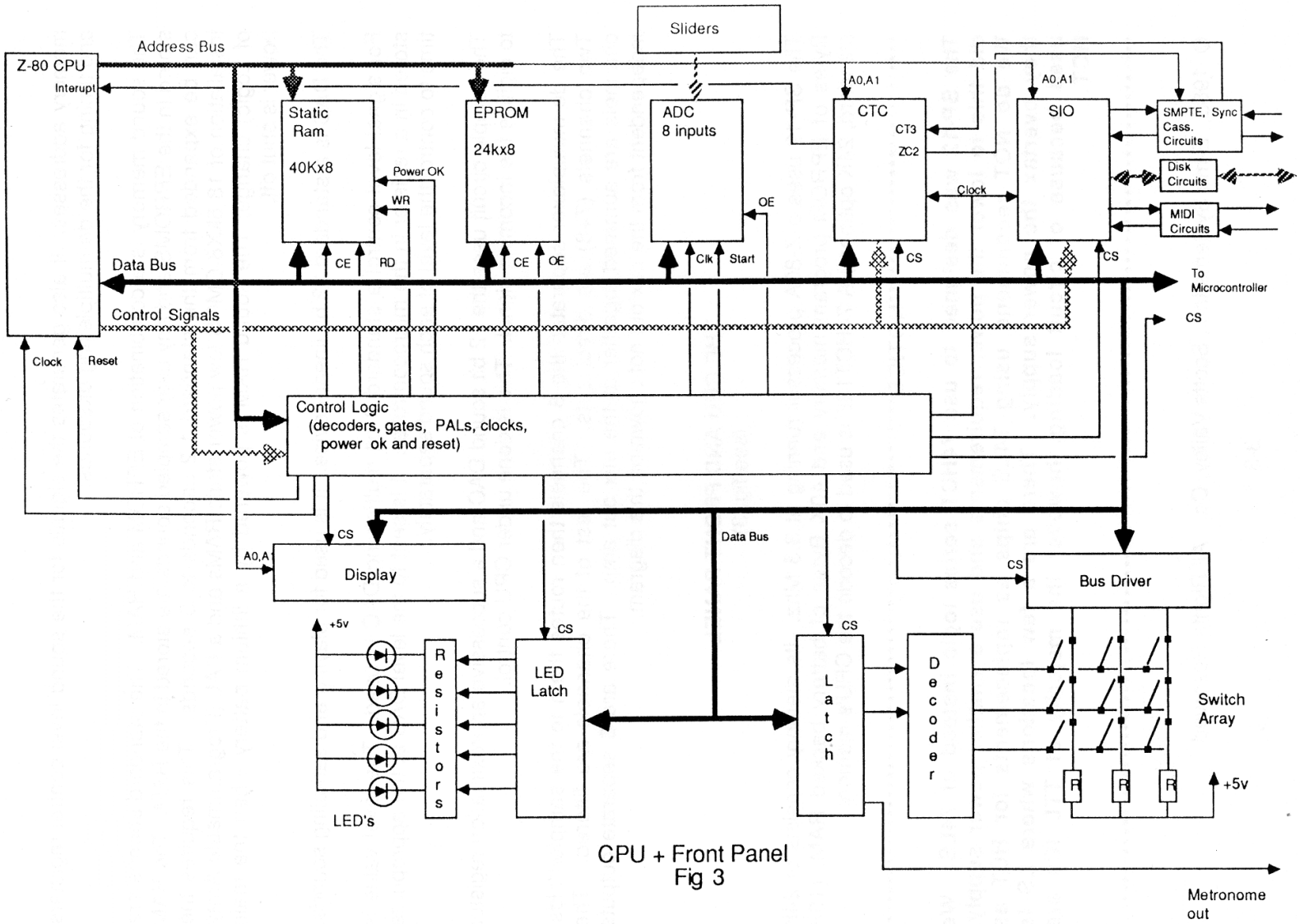


CPU + Front Panel
Fig 3

The ADC is a single chip. It has 8 analog inputs, 3 digital select lines to decode 1 of the 8 inputs, a clock input, a start conversion input, an end of conversion output, and an output enable. The ADC is mapped into two of the Z-80's I/O ports. The first port is written to select the 1 of 8 sliders and start the conversion. The second port is used to read back the digital value of the pot. Slider 8 is multiplexed with the dynamic button circuit on the front panel (see schematic page 3 of 4) using a 4053 analog mux. The ADC reads the output of this circuit and sends it to the CPU to control the playback level.

The CTC (Counter Timer Circuit) is used primarily for interrupt driven timing functions in the software. The most often used timing function is for what we call housekeeping. This is a interrupt generated by the CTC every 1.2 milli- seconds that reminds the CPU to read the front panel buttons and sliders. The second most often used CTC function is running the sequencer. If you look at schematic page 2 of 21 you will see that ZC2 (Zero Count channel 2) is connected to CT1 (Clock Trigger channel 1). This is done to cascade the two counters to provide very high resolution (.1 BPM) sequencer timing. The CTC is also used to generate a clock for the bit rate on the SMPTE/SYNC input. Lastly the CTC provides a transmit clock to the SIO (Serial Input Output) for outputting SMPTE and click signals.

The SIO (Serial Input Output) is used for all serial interfacing. It sends and receives all the signals for MIDI,SMPTE, CASS, Sync and the disk drive. As mentioned above the CTC supplies the SIO with a clock for signal rate control of SMPTE. Channel A is dedicated to MIDI, with conventional MIDI input, output and thru circuitry. Channel B is dedicated to the SMPTE/SYNC/CASS interface. The remaining pins on the SIO are used for implementing a Commodore disk drive interface. The SMPTE bi-phase decoder has two rates selected by the SIO's DTRB bit. Referring to schematic page 2 of 21 pin 25 of the SIO is connected to Q1 through R31. When pin 25 is high Q1 is off. This causes IC94's output pulse width to be determined by R41 and C81. When SIO pin 25 is low Q1 is turned on which causes R37 to be in parallel with R41. This changes the RC time constant on IC94 which narrows the pulse on its output. This is done to accomodate the two different SMPTE rates. The CASS/SYNC/SMPTE input (page 7-16) has two different sensitivities set by the signal +SMPTE.D. When this signal is high pin 2 of IC 104 is at 2.6 volts. An input signal as small as 250 mv will now change the state of IC 104's output. This circuit functions like a comparator taking a small analog signal and converting it to a square wave with digital levels. When the +SMPTE.D is low the circuit acts like a normal digital gate input which takes about 3 volts to trigger it. Following this circuit is an edge detector. This generates a 25 µS pulse on the rising or falling edge of the square wave input. The output of this circuit feeds a 1 shot whose pulse width is set by Q1 which was previously explained.

To better understand the SMPTE circuit see fig. 4, which is a timing diagram of the circuit on schematic page 2 of 21. The top of the diagram shows the bit cell time. Notice that a transition during a bit cell time indicates a 1 whereas no change is a 0. This is the standard SMPTE encoding scheme. The transition is a flux change on the tape. The signal recorded onto the tape is a square wave with 2 frequencies. One frequency is twice the rate of the other during a bit cell time. This is called bi-phase encoding. The higher frequency will cause a transition during the bit cell while the lower frequency will not. The top trace is the signal that came off the tape after it has been cleaned up by IC104. Compare this to the data at the SIO and you can see how the flux changes correspond to the data. The second trace is the output of the edge detector circuit. It can be seen that this circuit puts out a pulse, the width determined by R72 and C107, for every transition of the input signal. This signal is used to drive the 1 shot (IC94) and clock the flip flop (IC95) to qualify the data. If the edge detector output is high during the middle of a bit cell time, it clocks the 1 shot data into it. This is decoding a 1. If there is not an edge detected during the bit cell then the flip flop does not get clocked during the bit cell time and the output is a 0.

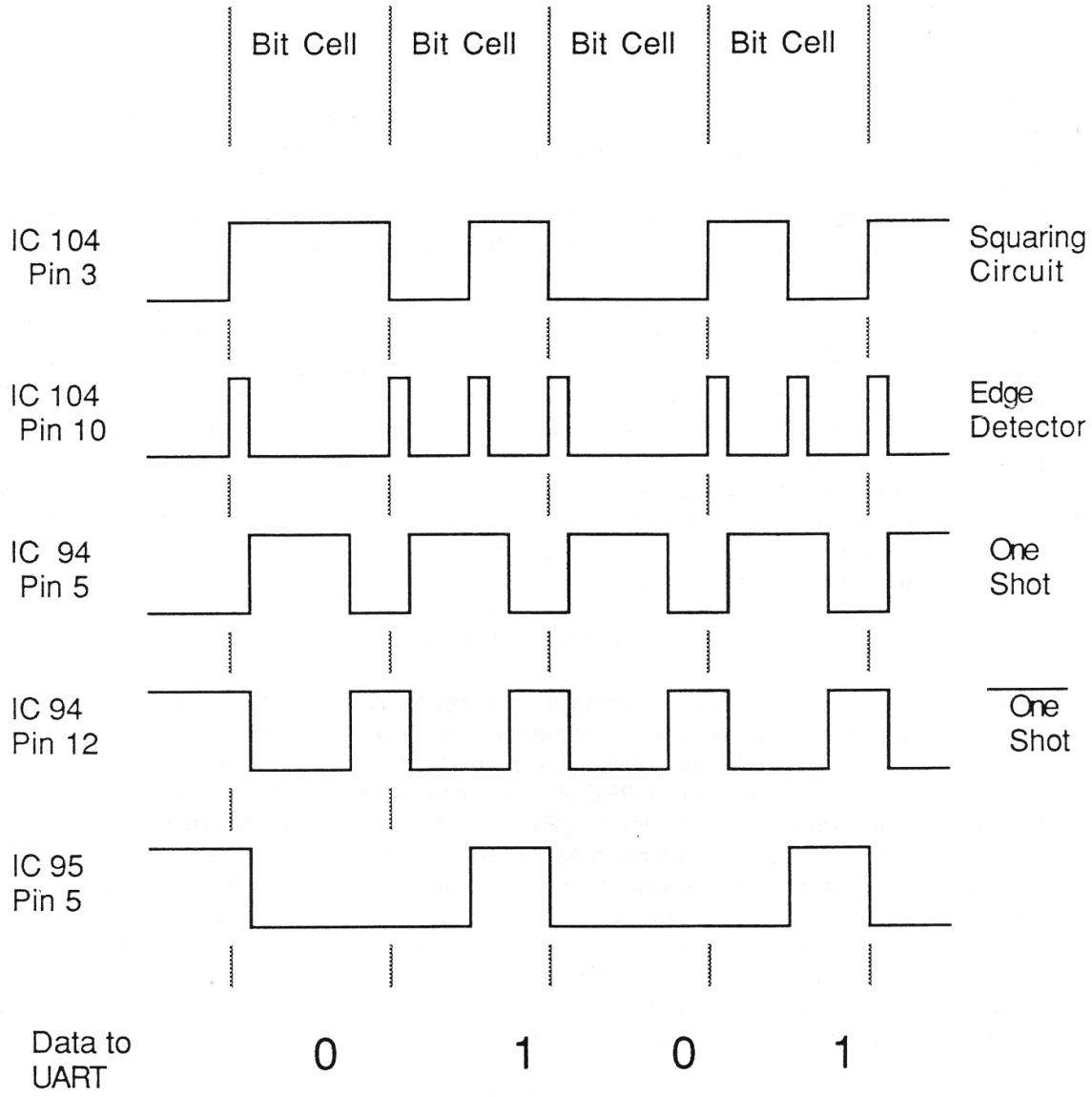
The external disk drive is interfaced using the remaining unused pins on the SIO to form a bidirectional serial bus that conforms to the Commodore standard. This can be seen on schematic page 2 of 21. Notice that the SIO inputs are connected to the interface outputs on the CLK and DATA signals. This is an inexpensive bidirectional bus. It works because the drivers are open collectors and their outputs are turned off when a 1 is on the input. This allows multiple drivers to be connected to one wire. The protocol is set up such that only one driver has the bus at any time. The input to the disk drive uses a similar arrangement. The disk uses 4 signals to interface with the SP-12. They are:

Disk Atn: The SP-12 uses this signal to start a command sequence. When this signal is brought low the disk listens for a command. If the disk does not respond, the SP-12 assumes no disk drive is connected.

Disk CLK: This clock is used for timing the data sent on the serial bus.

Disk Data: Serial bi-directional data bus

Disk SRQ: This signal is brought low when the disk wants to communicate with the SP-12.



SMPTE TIMING

FIG 4

The LEDs are mapped into the CPU's I/O space as a write only port. The LED latch is connected directly to the data bus. The CPU writes a 0 to the latch to turn the LED on and a 1 to turn it off. The resistors prevent excessive current flow through the LEDS.

The display is connected directly to the data bus and is mapped as an I/O port. After the display is initialized, the CPU sends ASCII character codes to it for displaying user messages.

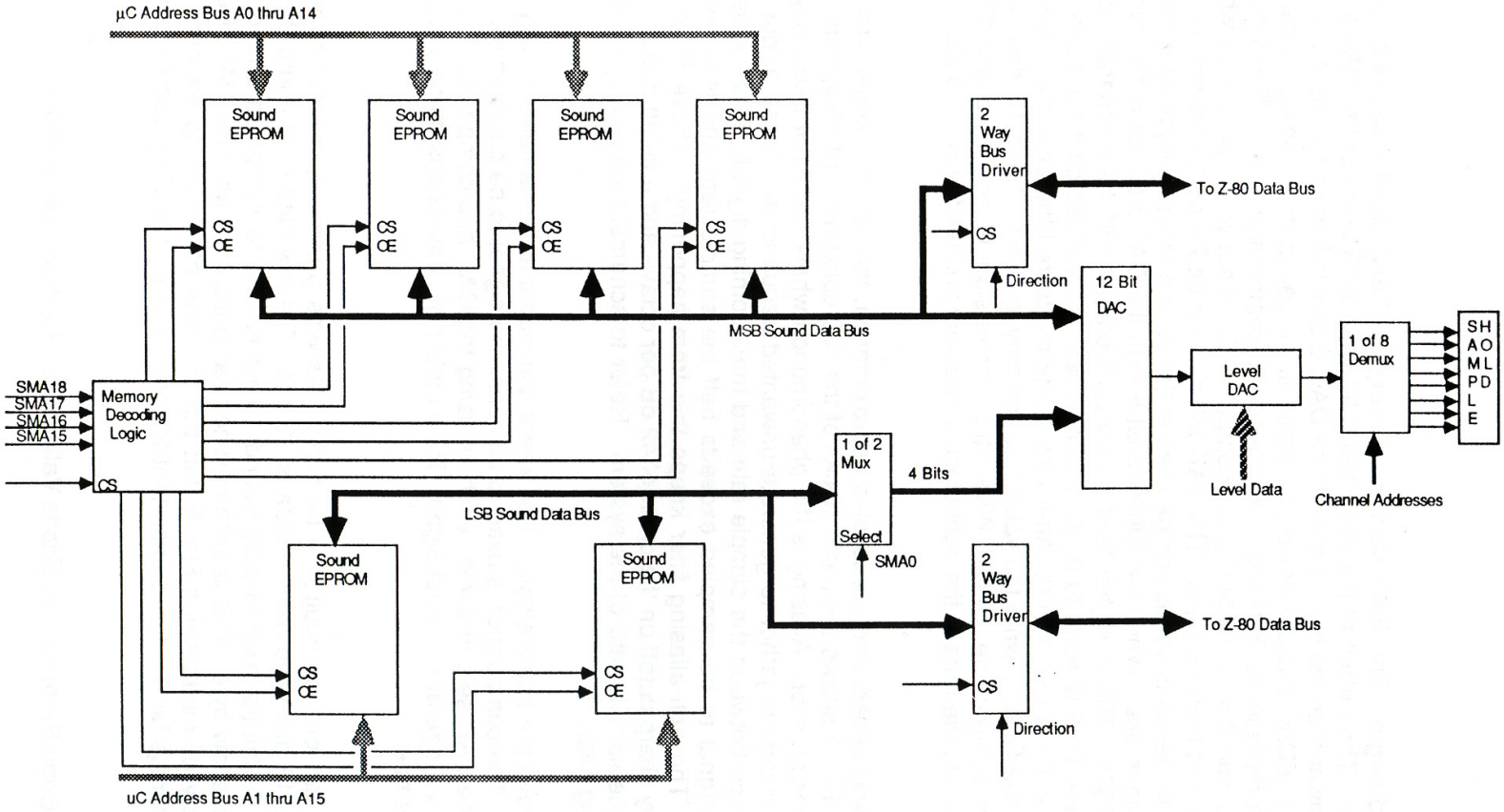
The buttons are arranged in a matrix as can be seen in fig. 3 The buttons are also mapped in the CPU's I/O space. When the Z-80 wants to read the buttons it writes to the button latch which drives a decoder which selects a row. The decoder's output goes low for the selected row. The colums are pulled up with resistors. If a switch was pressed in the selected row the column line would be pulled low and the decoder would sink the current. The CPU then reads the I/O port which selects the button bus driver. If any output of the bus driver is low then the button on that column (and the previously decoded row) is being pressed which will be read by the CPU and cause it to play a sound if a play button was pressed.

MEMORY DE-MULTIPLEXING

The SP-12 uses 12 bit linear encoding for the sound data. The sound memory is 16 bits wide but the low byte is de-multiplexed into two 4 bit nibbles each one used separately. To better understand this system see fig. 5. The top EPROMS are the most significant bytes while the lower EPROMS split their bytes with a de-multiplexer to form the least significant nibble. The lower EPROMS do not have an address 0 line. This causes data to be output half as often as the upper EPROMS. In other words, for every 2 bytes of data read from the upper memory only one byte gets read from the lower memory. The low memory's output goes to a 2 to 1 4 bit de-multiplexer strobed by address line 0. The first high byte and the low nibble of the low byte are sent to the DAC. Then the second byte of the high memory and the high nibble of the low byte are sent to the DAC. The bi-directional bus drivers that allow the main CPU to read and write to the sound memory can be seen on this diagram.

SAMPLING

The block diagram of the sampling circuits can be seen in fig. 6. The SP-12 uses the successive approximation technique to digitize the incoming audio signal. Before we get into the way the SP-12 samples, an explanation of successive approximation is in order. Referring to the top of fig. 6 the 3 most basic elements can be seen. They are: the DAC, a comparator and the SAR. (Successive Approximation Register) we intentionally left out a few details such as the CPU and sample/hold to simplify the drawing. To start the process the CPU would send a start conversion signal and the



Memory De-Multiplexing Diagram

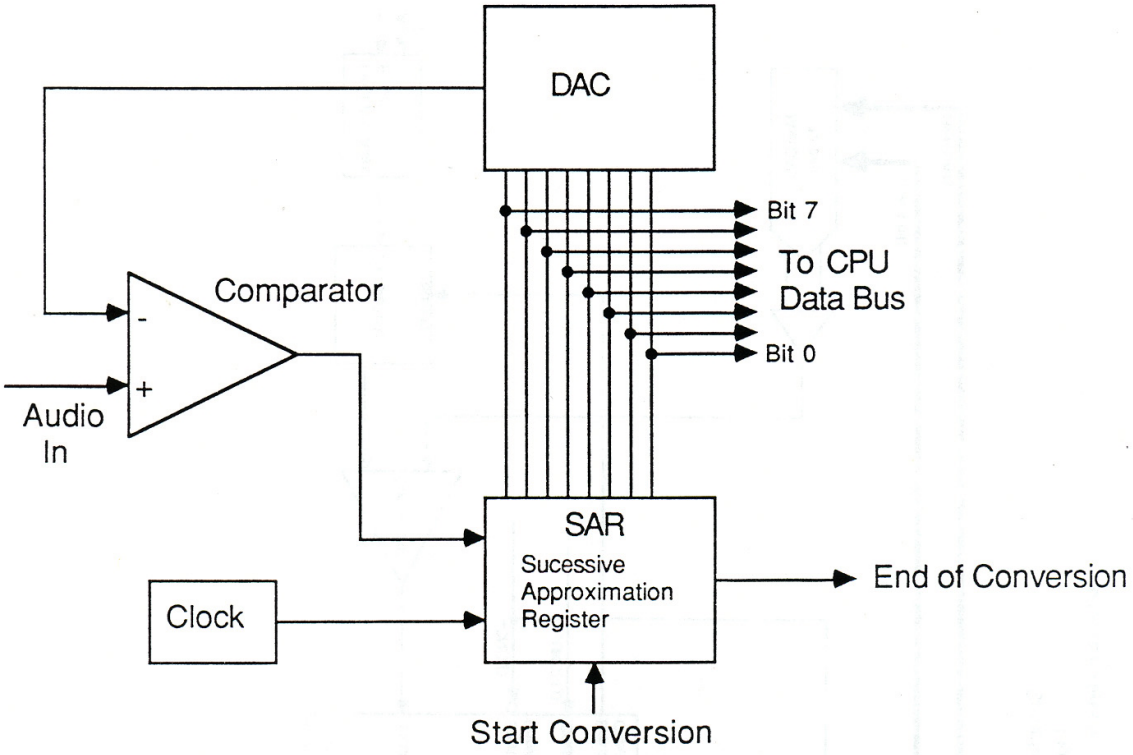
FIG 5

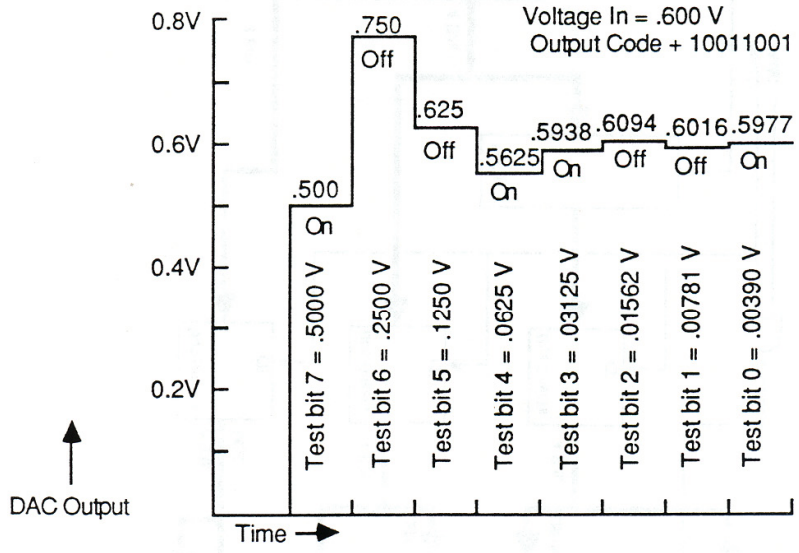
SAR would begin. The SAR starts by setting bit 7 and looking at the output of the comparator. The output of the comparator tells the SAR whether the DAC's output is higher or lower than the input signal. If the DAC output is higher, the input the bit will be set to 0. If the DAC output is lower, the input bit will be set to a 1. In fig . 6 the SAR set bit 7 which represents .500 volts and tested the comparator output. Since the + input was .600 V and the - was .500 V the comparator's output was high or true which says the DAC is less then the input. The SAR will now set bit 7 high for the remainder of the test. Next bit seven is set as can be seen at the bottom of fig. 6; each bit is exactly half of the previous one. When the SAR set bit 6 high the DAC's output is the sum of bit 7 and 6 or .750V. This is higher than .600 V on the input and the comparator output will be 0 or false. Bit 6 is reset to 0. As can be seen this process continues until all 8 bits are tested and set to a 1 or 0. After all the bits are tested the end of conversion goes true to tell the CPU to write the value to a memory location. The SAR does the actual conversion without the CPU. When the conversion is complete the CPU must intervene to put the data in the right place in memory and tell the SAR to start again.

Now that you understand successive approximation, the SP-12 sample circuit can be analyzed. Fig. 7 shows the basic blocks of the A/D converter. Starting from the left is the anti-aliasing filter. Aliasing is the phenomonon where the input frequency and the sample rate beat together to generate unwanted frequencies. These frequencies are the difference between the sample rate and the incoming signal. This happens when the input signal to be sampled exceeds half the sample rate and is allowed to be sampled. The anti-aliasing filter keeps this from happening. These filters usually have a very sharp cutoff on the order of 42 dB per octave and a cutoff frequency of less than half the sample rate of the system. Refer to schematic page 7 of 21 to see the anti-aliasing filter.

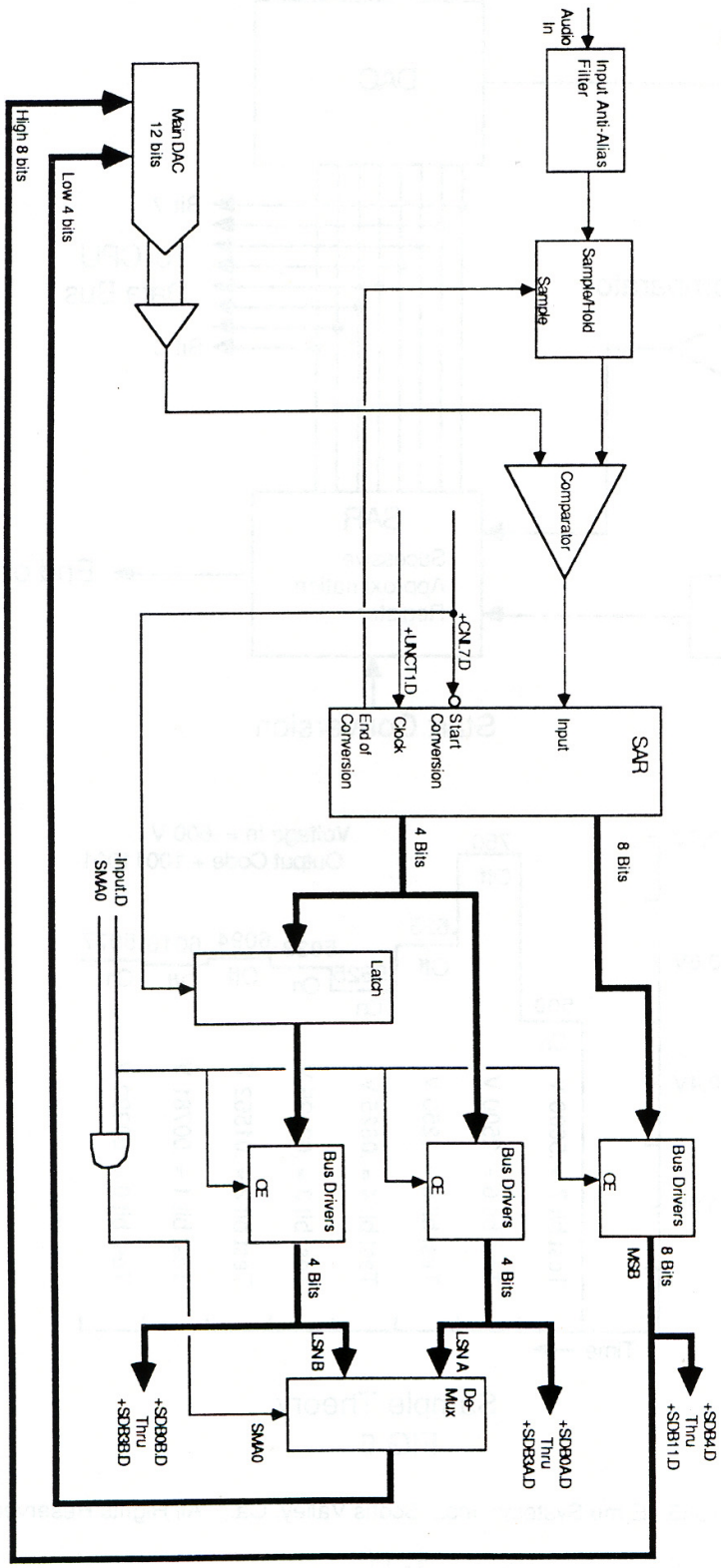
Next we have the sample/hold. This keeps the signal to be sampled steady while we convert it. The comparator is used to compare the signal to be sampled with the DAC output. The SAR sets and tests each bit using the DAC and comparator to determine the actual voltage of the input signal. The number of conversions made per second is the sample rate.

The next part of the circuit is a bit tricky. As was previously mentioned the sound memory is 16 bits wide but the data is 12 bits. The low byte is split into 2 nibbles (4 bits) and de-multiplexed to play sound. This means to sample a sound we must multiplex the low byte. This is accomplished using the latch after the DAC. Recall from the memory de-multiplexing Fig. 5 that the low byte of the sound memory does not have a address bit 0. This is important to remember so sampling can be understood. This





Sample Theory
FIG 6



Sample Circuits
Fig. 7

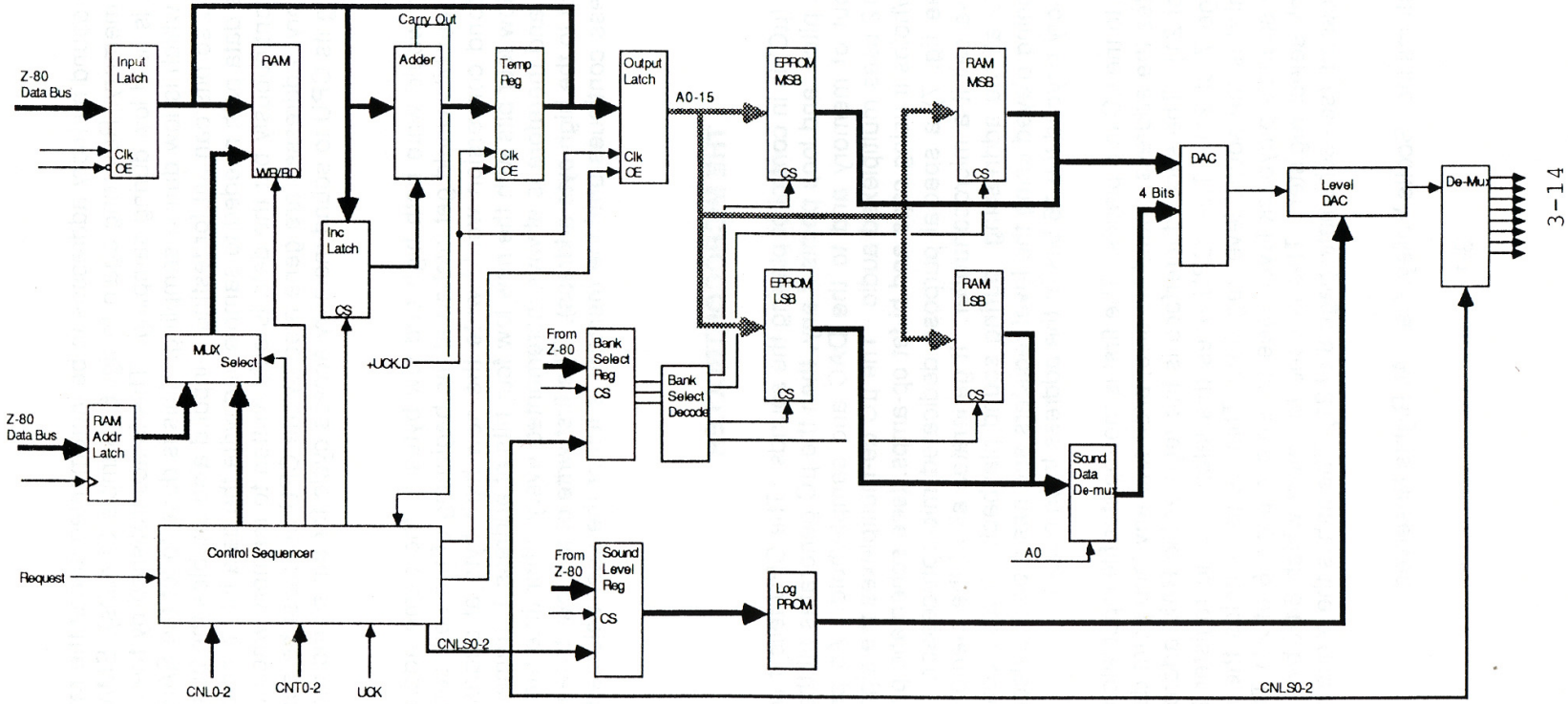
causes the low byte sound memory addresses to be incremented at half the rate of the high byte of sound memory. Referring again to fig. 6 (Sample Circuits), SMA0 which controls the de-mux is held low during sampling. This is acomplished by the and gate and signal -input.d, which is low during sampling. This is done to let the SAR have a data path to the DAC so bits can set for testing. -input.d also enables the bus drivers, which completes the data path needed to sample and write the data into memory. The SAR is converting continuously but the data is only written to memory when the CPU allows it. The memory addresses are generated by the CPU but must be sent to the microcontroller during its CPU to sound memory access cycle for the sound memory to be addressed.

The first conversion would write both high and low bytes to the same address, say address 1. The low four bits would get latched at the beginning of the next conversion. The end of the second conversion would write the new high byte at address 2 but would write the old low four bits with the new low four bits at address 1. (remember the low byte has no A0 and therefore is always incremented every other time the address changes with respect to the high byte address). The first write of the low byte is always garbage. This process continues until the memory is full or the user selected sample time has ended.

THE MICROCONTROLLER

The Microcontroller (μC) is in control of playing the sounds. The CPU tells it where the sound is, the lengh, pitch and loop points if any, then the μC generates all the signals to get the sound out of memory and to the DAC and sample/hold. As previously mentioned the SP-12 uses multiplexed audio. The μC de-multiplexes the signal using a 4051 and sample/holds it using caps and bi-fet op-amps. (see schematic page 18 of 21) The μC is (see fig. 7) a special purpose dedicated microprocessor. It is not programmable so we call it a microcontroller. It generates all of the memory control signals and handles all the addressing during sound playback. It also controls the level of the sound being played using the level registers and has a bank select register for addressing memory beyond the 16 bits of the address latch output.

The Z-80 interfaces to the μC in 5 places. The first is the register file input latch. This is where the CPU writes the address, sound file size, pitch and any loop point data. (see schematic page 9 of 21). The second interface is the register file RAM address latch. (see schematic page 7 of 21). The CPU uses this latch to load register file RAM addresses. The third is the sound level register. This register holds the data that corresponds to the sound's playback level. (see schematic page 8 of 21) The fourth interface is the bank select register. This is used to select which 64K byte block of memory will be accessed. (see schematic page 8 of 21) The fifth is the request latch.



Microcontroller
FIG 8

This is set after the CPU has loaded data in the register file input latch and the register file RAM address latch. When the μC reads this latch it knows that data is in those latches and writes it into the register file RAM. (See schematic page 7 of 21, IC 60) Referring to fig. 7 the five interfaces can be seen. The actual data is right off the Z-80 data bus. The CPU writes to the μC as 5 separate I/O ports.

POWER SUPPLY

The SP-12 uses a linear power supply to generate all the necessary voltages. The transformer, power switch, 115/220 switch, fuse and diode bridge are mounted on the back panel and can be seen on page 7-36. The transformer has 2 secondaries. The lower secondary is a 36 volt AC center tap which is rectified by D3 thru D6, (see schematic page 21 of 21) filtered by C85 and C77 and regulated to +- 15 volts by VR1 and VR2. The other secondary is 12 volts which is rectified by the diode bridge, filtered by C153 and regulated to +5 volts by the 3 terminal IC regulator VR4. Additionally VR3 supplies the +5 volts to all the non-volatile RAMs when AC power is present. When the main AC power is off D11 reverse biases and D13 forward biases to supply the RAMs with about 3 volts for memory retention.

The power OK circuit (schematic page 21 of 21) is used to generate a raw reset signal for the CPU and to disable the battery powered RAM during power up and down. The circuit uses transistor Q4 and zener diode D1 to sense the voltage of the unregulated +5 volt supply. When the power is stable Q4 turns on which turns off Q3. Q3 turned off turns on Q2 and connects +PWROK to the 5 Volt supply. If the unrequlated +5 drops below 6.2 volts Q4 turns off and Q3 turns on which causes Q2 to turn on and +PWROK is effectively grounded.

SECTION 4

MECHANICAL PROCEDURES

REMOVING THE TOP COVER

Before taking the SP-12 apart we recommend providing a soft work surface. When the machine is in the service position the front panel will be face down on the work surface which might damage it. We also recommend the use of an extra long interpanel cable (50 pin ribbon) which will allow you to place the top panel face up next to the bottom panel. This will prevent top panel scratches while allowing access to the front panel and the main PCB inside the machine.

To open the SP-12 lay it upside down on a soft surface and remove the 5 screws on the bottom panel. Flip the machine right side up and remove the 3 back panel screws. Position the SP-12 such that you are looking at the right side of it. Grasp the top panel at its thickest portion and lift it as though there was a hinge at the front. This is analogous to opening the cover of a large book. The top cover will pivot about 180 degrees and lay face down on the work surface. The front panel PCB is connected to the main PCB via a short 50 pin ribbon cable. This cable can be removed from either or both ends. As previously mentioned replacing this cable with one that is about 2 feet long will make working on the machine much easier. These cables can be found at electronics and computer stores or through mail order.

REMOVING THE FRONT PANEL PCB

First remove the 50 pin ribbon and audio cables. Next remove the knobs from the front panel. Lay the top cover face down on a soft work surface and remove the 12 screws and lift out the PCB. If any parts need replacement the fisch paper will have to be removed. Note the inside of the top cover is coated with a conductive material. The fisch paper keeps the circuitry from shorting to this coating. To install the PCB reverse the above procedure.

REMOVING THE MAIN PCB

Unplug the 50 pin ribbon and audio cables. Remove the nuts and washers on the back panel jacks. Unplug the AC harness from the PCB. Remove the screw, nut and washer that hold the 3 terminal voltage regulator onto the back panel. Remove the 8 screws holding the PCB in place and remove the PCB carefully. To install, reverse the above procedure. After installing the PCB check for a lack of continuity between the 3 terminal regulator's case and the back panel. Also a little dab of heat sink compound on the regulator prior to re-assembly is recommended.

SECTION 5

SP-12 FUNCTIONAL TEST

This functional test is designed to test all of the functions without taking the machine apart. Everthing can be tested using this procedure but it is not as quick and in some cases not as thorough as using the debug EPROM. (see section 6) The debug EPROM will overwrite any data in memory which the owner might not appreciate. It is a good idea to tell the owner to make copies of all sequences and sounds before the machine is worked on. If that isn't possible you should make copies because some of the tests that are performed will change the memory.

You will need a pre/power amp or receiver with a speaker or headphones to accomplish the functional test.

Following the functional test is a trim procedure. If the sound tests have questionable results the trims could be the culprit.

***************************WARNING***

THE INDIVIDUAL CHANNEL AND METRONOME OUTPUTS ARE ALWAYS AT FULL LEVEL. SET AMPLIFIER ACCORDINGLY WHEN LISTENING TO THESE OUTPUTS.

****

1. **LED Test.** All the LEDs are turned on for a couple of seconds when power is first applied. Check to see that all of them are lit.

2. **Display.** The display has 2 lines of 16 characters. If you can read both lines of the sign on message the display is probably OK. The sign-on message on a turbo machine with version 2.1 of software looks like this:

   SP-12 Turbo
   Vers 2.1 9/26/85

   Press Set-up. The display should read:

   Set-up Function?
   [11-23]

   We haven't seen many display failures, and don't expect you will see problems

very often. If one fails just replace the whole assembly and return the old one.

3. **Button Test.** Test the sound buttons by pressing each one and listening for a sound. Hit the button hard and the sound will get louder. If it does not the dynamic button circuit could be at fault . Test the SELECT button by pressing it and looking to see if the LED that is lit is advanced by one. The TUNE/DECAY and SONG/SEGMENT buttons are tested similarly. Press the Set-Up button and check that it's LED comes on. The Cassette/Disk, Sync and sample buttons are tested the same way. To test the TEMPO button press Song/Segment button to get into either one of those modes. Press TEMPO and check that the blinking cursor on the display is now under the tempo value. Now press the left arrow button and check that the tempo value decreases. Press the right arrow button and the tempo value should increase. Press the ENTER button and the blinking cursor on the display will move to a position under the song/segment number. Pressing any keypad button twice will change the song/segment number to a two digit value corresponding to the button pressed. To test the tap/repeat button press and hold it then press any sound button and listen for the sound repeating continously. The rate of repeat will be determined by the auto correct setting. Test the RUN/STOP button pressing it while in segment mode. One of two things should happen. If the segment selected has a sequence in it, the SP-12 will begin playing. If the segment was empty the metronome will beep. To test RECORD get into SONG mode by pressing the SONG/SEGMENT button. Now press RECORD and the LED should light.

4. **Sound Test.** You should listen to all the sounds critically at the mix out jack and at their separate output jacks. Plugging into the separate outputs will remove that sound from the mix output. Listen for excessive noise or distortion, clicks or pops and any other abnormalities. If any one or two sounds are bad, check to see if they share an output channel. If they do that channel's output filter or sample/hold is suspect. If all sounds are bad check the separate channel out. If they sound good here then the mix amp is suspect. If they are still bad check the main and level DACs and their buffers. If nothing looks bad the debug EPROM should be installed so the sound memory and sound quality tests can be run. Also listen to the metronome output by plugging into the met jack and running a sequence. This is a full level output so be careful.

5. **Slider Test.** Press the tune decay button twice to call up mix mode. The display will show a bar graph for each slider corresponding to the sound level during playback. Before testing the sliders note the position of the bar graph so it can be restored to original. Test each slider by moving it to the maximum and minimum position while watching the display. At minimum only one segment will be seen. At maximum all the segments in the bar will be seen. Adjust the slider until the bar

graph is returned to the original position. Test the remaining sliders the same way.

6. **Potentiometer Test**. To test the mix out pot start a sequence by pressing RUN/STOP. Turn the pot through it's full range listening for noise or dropout. Test the metronome pot by creating a segment with no sounds playing. To do this find a blank segment or erase one. Press record and hold it, then press RUN/STOP. You will now hear the metronome clicking at quarter note intervals. Turn the metronome pot through its full range listening for noise or sound dropout. When the pot is at minimum no metronome should be heard.

   To test the sample pot it will be necessary to erase some of the sample memory. If the sound in the sample memory is valuable to the owner then it should be backed up by saving it tape or disk. If possible have the owner do this. To erase sound memory press Set-up, 23, 15 and yes. This will erase all of the sound memory. Now press sample. You will need a signal source to sample to accomplish this test. The radio, a synthesizer or a signal generator will work. Connect the audio source to the sample input. Press sample and adjust the input level by pressing 3 and then using the right and left arrow select 0, 20 or 40 dB. Set the input level so the gain pot can be at maximum and the VU meter does not go off scale. Press 9 to start sampling and turn the sample pot from its maximum to minimum during the sampling period. If the machine is not expanded the sample will take 1.2 seconds. If the sound memory is expanded the sample will be 2.5 seconds long. Press sample to exit the module. Press SELECT next to the play buttons until LED 4 is lit. Play the User 1 button and listen to the sample. Listen for a steadily decreasing level with no pops clicks or sound droupout.

7. **Disk Test.** You will need a Commodore disk drive to test the disk interface. Connect the drive using the Commodore disk cable. Put a blank disk in the drive. Press Cassette/Disk, 20 and ENTER. The drive will format the disk. The best way to test the read/write capability of the disk is to save a sampled sound. If the machine has the turbo kit and sound memory is full it will take two disks. We recommend a sample length of 1 to 2 seconds to keep the test from taking too long. The sound memory can be erased by pressing Set-up, 23, 15 and yes. Now take a sample no longer then 2 seconds. Go back to the Cassette/Disk module and save sounds (22). This will take about 3 minutes. To complete the test erase the sound memory (see above) and load the disk back in. Listen and make sure the sample sounds OK.

8. **MIDI Test.** To test MIDI a keyboard or drum machine that is MIDI equipped will be needed. Connect the SP-12's MIDI out to the other machine's MIDI in. (ex: a DX-7) If using a keyboard select a patch that has a fast attack on the envelope. Hit a few play buttons on the SP-12 while listening to the other machine. Does it play?

If it does the SP-12's MIDI transmit is OK. Now connect the SP-12's MIDI in to the other machine's MIDI out. Play a few keys or buttons while listening to the SP-12. If it plays the MIDI receive circuits function properly. If this test fails try running the MIDI test using the debug EPROM. (see section 6)

9. **Cassette Test.** You will need a tape deck to perform this test. Because the tape save takes a while we'll save sequences instead of sounds. Plug the CASS jack out to your tape deck in. If the SP-12 does not have sequences in it you will need to create some. Select segment mode, press and hold record then press RUN/STOP. You can now play a pattern and it will be recorded. To save it start the tape recording then press Cassette/Disk, 11 and enter. The display will tell you when it is finished. Now we need to erase the sequencer memory and load the sequence back in. Press Set-up, 23, 16 and yes. Rewind the tape, connect tape out to the SP-12 CASS in. Press Cassette/Disk, 13 then ENTER. Start the tape in play mode. If this test does not work try adjusting levels on the tape deck or you could test the interface using the debug EPROM.

10. **SMPTE Test.** You will need to use a tape deck for this test. We will write a SMPTE track on the tape, rewind the tape and trigger the sequencer with the SMPTE track we just made. Plug the SP-12's SMPTE out jack into your tape deck input. Start the tape recording. Press Set-up, 23 and 14. Adjust the record level to -3 VU. Let it run for about a minute. Press ENTER to stop the SP-12 and rewind the tape to the beginning. On the SP-12 press Sync, 3, then press ENTER 3 times. Get into segment mode and press RUN/STOP to play a segment. The display should tell you it's "Awaiting SMPTE". Plug the tape deck output into the SMPTE input. Start the tape and watch the display. When SMPTE is received and decoded the display will change and replace the "awaiting SMPTE" message with the SMPTE time display which shows:

    00:00:00:00

    The numbers represent hours, minutes, seconds, frames. The frames will be changing fast enough to be difficult to read. The debug EPROM also has a SMPTE test. (see Section 6)

11. **Sync Test.** The SYNC input uses the same circuits as the CASS input. The CASS read/write test is a better test of these circuits so we suggest that you use that test.

12. **Non-Volatile Memory Test**. To run this test sampled sounds and sequences must be in memory. If there are sounds and sequences in the machine listen to

them so you are familiar enough to identify them. Turn off the power and wait a couple of minutes. Re-apply power and listen to the sounds and sequences and see if they have changed. The debug EPROM has a very good test for this.

13. **External Footswitches.** You will need a footswitch that terminates with a 1/4" plug. Alternately any 1/4" cord can be used and one end can be shorted using a suitable conductor. Plug into the RUN/STOP jack. This should start and stop the sequencer when the footswitch is pressed. Plug into the STEP/END REPEAT jack. Press the song segment button to get into song mode. Watch the display while you press the switch and you will see the song number advance. Plug the footswitch into the TAP/AUTO REPEAT jack. Press and hold the footswitch while holding down a play button. The sound should retrigger continuously as long as you hold them down. The debug EPROM also has a test for these jacks.

TRIM PROCEDURES

The SP-12 has 6 trimmers located on the main circuit board.Three of them are trimmed with a digital voltmeter using analog ground and the test points listed below. The other two are trimmed using an oscilloscope or frequency counter connected to the mix out. The remaining one is trimmed using the Debug EPROM. The first 4 trimmers should be trimmed in the order they are listed below. RT5 and 6 can be trimmed anytime. We recommend trimming the machine after it has been on for at least 15 minutes.

TRIMMER	TEST POINT	SPECIFICATION
RT2	IC98 Pin 2	Less Than 5 Millivolts
RT3		Less Than 1 Millivolt
RT4	IC99 Pin 6	Less Than 1 Millivolt
RT1	The Debug EPROM is used. See Section 6.	

RT5 and 6 are the dynamic filter trims and need to be trimmed with an oscilloscope or frequency counter. The filter's Q is increased to the point where the filter oscillates by shorting two test points together located just to the left of the respective trimmer. The frequency of oscillation is adjusted to 1.3 Khz (760 microseconds) using the trimmer.

POWER SUPPLY SPECIFICATIONS

The SP-12 has 5 voltages that need to be within specifications. They are:

VOLTAGE	TEST POINT	SPECIFICATION
+5V Digital	IC18 Pin 20	4.75 to 5.25 Volts
+5V Non-Volatile	IC1 Pin 2	4.75 to 5.25 Volts
+15V Analog	IC113 Pin 4	14.25 to 15.75 Volts
-15V Analog	IC113 Pin 11	-14.25 to -15.75 Volts
WITH POWER OFF		
+5V Non-Volatile	IC1 Pin 2	No less then 2.5 Volts

SECTION 6

INSTRUCTIONS FOR SP-12 DEBUG EPROM VERSION 1.6

The debug EPROM is a tool designed to help the technician debug the SP-12. It includes tests for memory, external interfaces, buttons, LEDs, the display, sliders, RAM, sound and sound data bits.

To make life easier when working on the SP-12 we suggest you get a 50 pin ribbon cable that is about 2 feet long to connect the main PCB to the front panel PCB. This will allow you to access the front panel and the inside of the machine at the same time. A computer supply store is a good place to find one of these.

The Debug software is written so the initial power up sequence uses the minimum number of ICs and circuits. This is done to simplify troubleshooting a machine that has a microprocessor that is not able to work correctly through no fault of it's own.

Following is a list of the devices that need to work before the debug EPROM can boot. Their schematic page reference is also listed.

Main Digital ICs

Z-80 CPU (IC107) Pg. 1 of 21
EPROM (IC114) Pg. 3 of 21
74LS138 (IC110) Pg. 3 of 21
74HCT08 (IC109) Pg. 3 of 21

Reset and Power OK devices

74LS14 (IC83) Pg. 1 of 21
Q2, Q3, Q4, and D1 Pg. 21 of 21

Clock Circuit

74S04 (IC78) Pg. 1 of 21
74HCT74 (IC79) Pg. 1 of 21
74LS190 (IC77) Pg. 1 of 21
74HCT163 (IC80) Pg. 1 of 21

To use the Debug EPROM, substitute it for IC114 and apply power. It boots with the following sequence:

1. Flash all LEDs 3 times
2. Display "Testing Memory" while it tests the sequence memory
3. Reports any errors.
4. If no errors occurred the following sign-on message is displayed and the program waits for a user input.

NOTE: An asterisk (*) after the testing memory message indicates expanded memory option is being tested.

Diagnostic 1.6
Enter Test #

The test number (01, 02 ... 16, 17) is entered and the test will begin. Leading zeros must be entered for the test to work. To exit any test press the ENTER button.

Following is a list of the tests. A complete description of each test follows this list.

DEBUG EPROM TEST NUMBER ASSIGNMENT

01. Button Test
02. Slider Test
03. Display Test
04. LED Test
05. CTC Tests
06. SIO Test
07. Sound Memory Test
08. Metronome Test
09. Footswitch Test
10. MIDI Test
11. Cassette Test
12. SMPTE Test
13. Sound and Bit Test
14. NV Memory Test

15. DAC Trim
16. Dynamic Buttons
17. Disk/SMPTE Test

BUTTON TEST 01

This test will display the name of the button pressed and the number of times it was pressed. The following message will be displayed after the test is entered.

Button Test 0

Pressing and holding the record/edit button changes the display to;

Button Test 1
record

If the button is pressed once and the number is incremented more than 1 time, it has a bounce problem and should be replaced.

Press ENTER to exit the test.

SLIDER TEST 02

This test displays the decimal value of the sliders. The range is 0 to 255. The value will normally jitter on certain settings but should not exceed +-2. If the test was activated with all sliders at maximum, the following display would be observed;

255 255 255 255
255 255 255 255

Make sure all the sliders have a range from 0 to 255.

Press ENTER to exit the test.

DISPLAY TEST 03

This test activates every pixel on the display. The display will have all of it's active areas darkened. Observe the display closely and check that all of the indvidual elements for each character are dark.

Press ENTER to exit the test.

LED TEST 04

This test turns on one LED at a time. Pressing the right arrow advances the test and lights the next LED. Below is the order in which the LEDs are lit.

Set Up
RECORD/EDIT
RUN/STOP
SELECT 1
" 2
" 3
" 4
MULTIMODE
MIX
TUNE/DECAY
SEGMENT
SONG
Sample
Sync
Cassette/Disk

Press ENTER to exit the test.

CTC TEST 05

This test has two parts, The first part tests the CTC to CPU communication. The second part, which is activated by pressing enter, tests interrupt and counting modes of the CTC. The test will report which, if any, of the four CTC channels failed. If the first test failed on channel 1 the following display would be seen

CTC R/W Test:
Channel 1 FAILED

If the test passed the display would read:

CTC R/W Test: OK

Pressing ENTER activates the interrupt and counting tests. A failure on channel 0 would cause the following display.

CTC Int Test:
Channel 0 FAILED

If it passed the previous test the display would show:

CTC Int Test: OK

Press ENTER to exit the test.

SIO TEST 06

This tests the SIO to CPU communication and displays any failure. A typical failure would be displayed as follows.

SIO R/W Test:
FAILED

The display for a successful completion of the test would be:

SIO R/W Test: OK

SOUND MEMORY TEST 07

This test checks that all of the sound memory locations have the ability to read and write. When the test is activated the following message will be displayed.

Testing Snd Mem

If a failure occurred the display would change to;

Snd Mem Error @
77FFF IC55 Bad?

If the test ran without any errors the display would read;

Sound Mem: OK

Press ENTER to exit the test.

METRONOME TEST 08

This test clicks the metronome every 600 milliseconds. Listen to the mix output to check

it. The metronome output can also be used. Be careful when using the metronome output as it is always at full level.

Press ENTER to exit the test.

FOOTSWITCH TEST 09

There are 3 footswitch jacks on the back panel that need to be tested. They are RUN/STOP, STEP/END REP and TAP/AUTO REP. Using a footswitch with a 1/4" phone plug on the end of it's cord, plug into each jack and press the switch while observing the display. The name of the footswitch pressed will be displayed to indicate the CPU successfully recognized it. Below is the display for this test when plugged into the TAP/AUTO REPEAT jack.

Footswitch Test
TAP

Press ENTER to exit the test.

MIDI TEST 10

MIDI in must be plugged into MIDI out for this test. This is a loop through type of test. A failure would be displayed as follows.

MIDI FAIL. In &
Out Unconnected?

If the test passed the display would show the following:

MIDI: OK

Press ENTER to exit the test.

CASSETTE TEST 11

Plug CASS in to CASS out. This a loop through test. A failure would be displayed as follows.

CASS FAIL. In &
Out Unconnected?

If the test passed the following display would result.

Cassette: OK

SMPTE TEST 12

SMPTE in must be plugged into SMPTE out to run this test. This is also a loop through type of test. A failure would be displayed as follows.

SMPTE FAIL In &
Out Unconnected?

When the test passes it displays:

SMPTE: OK

Press ENTER to Exit the test.

SOUND AND BIT TEST 13

The sound test will generate a 1 Khz sine wave on any output channel you choose. The bit test will increment through all the bits that go to the sound DAC. Using an oscilloscope missing bits can be found. When the test is started the display will show:

Select Test
1=Sound 2=Bit

Pressing 1 displays:

Select Output
Channel 1 to 8

Channels 1 and 2 are the dynamic filters. Channels 3 thru 6 are fixed filters. Channels 7 and 8 are direct outputs. Press 1 and you will get the following display.

Playing on
Channel 1

Test 2 also asks which channel you want to use and displays your choice while the test is in progress. When test 2 is running you can scope the DAC output and look for missing bits. The test increments all 12 bits one at a time to give a staircase output with 4096 steps.

Press ENTER to exit the test.

NV RAM TEST 14

This test writes a pattern into all the NV RAMs (including sound memory) and asks you to turn the power off. Leave the power off for a couple of minutes to let all capacitors discharge. Reapply power and the test will look for the patterns it left in memory. If any memory locations are bad the display will indicate them. If a failure occurred the display would read:

NV RAM Test:
Failed @ IC 55

If the test was successful the display would show:

NV RAM Test: OK

Press ENTER to exit the test.

DAC TRIM 15

This is for trimming RT1. It has been relocated and can now be found next to C65. Trim RT1 until the display reads 800.

Press ENTER to exit the test.

DYNAMIC BUTTONS 16

This test is for testing and trimming the dynamic button circuit. The circuit and trimmer are located on the front panel PCB. When the test is started the display will show:

Dynamic Buttons

Hitting a play button will change the display to:

Dynamic Buttons
180

The number corresponds to the amount of force used to press the button. You should get a range from 20 to 200. The trimmer adjusts the sensitivity of the circuit. The trimmer has been preset at the factory and generally will not need to be changed. If it is not possible to get 200 from a hard hit on the button turn the trimmer clockwise to increase the sensitivity. Conversely if a light hit on the button displays 200 or more turn

the trimmer counterclockwise to decrease sensitivity.

DISK/SMPTE PULSE WIDTH TEST 17

The Disk portion of this test is useful for testing the interface without a disk drive. We highly recommend using a real disk drive to do a functional test on this interface as this test does not reflect a real world situation. (see Section 6 for disk test information) When you call up test 17 the display will show:

Disk/SMPTE Test

The display will not change during the test. The disk portion of this test will require a scope or voltmeter and a clip lead for grounding test points. For the first test put your scope or meter on IC103 pin 3. It should be logic 1 at this time. Press play 8 (play 1) and check to see that the signal goes to a logic 0. When you press the play button the SELECT LED 3 will light.

**********NOTICE **********

On very early SP-12s the front panel board play switch layout is mirror imaged. This means that you would press play 1 for the above mentioned test instead of play 8. These PCBs can be easily identified by a piggyback PCB that contains the dynamic button circuitry. These machines also use a different software EPROM in the IC115 location. It will have a B1 on the label to indicate a revision 1 PCB.

****

Move your probe to IC103 pin 10. It will be at logic 1 until you press Play 7 at which time it will go to logic 0. The SELECT 4 LED will light for as long as play 7 (2) is held. Move the probe to IC103 pin 6 and check for a logic 1. Press play 6 (3) and see if a logic 0 is displayed. No LED lights for play 6. This completes the first half of the disk test. For the second half of the test you will need a jumper to short signals to ground. Connect one end of the jumper to a suitable ground. Touch the other side of the jumper to IC103 pin 8 which will cause SELECT 3 LED to light. Move the jumper to IC103 pin 10 and the SELECT 4 LED will light.

To test the SMPTE pulse width you will need an oscilloscope and a cable with 1/4" plugs on both ends. Plug the SMPTE in to SMPTE out and set the scope to 2 millivolts per division sensitivity and the sweep time to 50 microseconds. Probe IC94 pin 12 (see schematic page 2 of 21) and check that the pulse width is between 250 and 305

microseconds (μs) in duration. Now press play button 5 and hold it. This will turn off Q1 which changes the RC time constant on IC94 and will increase the pulse width. Check that the pulse width is now between 300 and 370 μs. If both of these tests fail it could be a C81 or IC94. If only one is bad check to see if Q1 is leaky.

SECTION 7

SCHEMATICS

E-mu SIGNAL NAME DEFINITIONS

If you look at the schematics it can be seen that every signal that goes off the page has a unique name. They might seem cryptic at first glance but are actually quite logical once you understand the system. Let's look at a typical name and dissect its meaning.

-WR.D

Starting from the left we see a minus (-) sign. This indicates the active state of the signal. Minus means active low or negative. WR is the name of the signal; in this case it stands for write. The dot (.) is a separator to indicate the end of the characters that represent the signal name. The D tells you what type of signal it is; in this case it stands for digital.

We have two signal types D and V. As previously mentioned D is for digital and the V is for voltage. V is used for all of the analog signals. If you are familiar with microcomputers and mnemonics most of the digital signals will be easy to figure out. Following is a partial list of digital signal name mnemomics with their full names.

MNEMONIC	NAME
A15	Z-80 Address Bit 15
D7	Z-80 Data Bit 7
MREQ	Z-80 Memory Request
IORQ	Z-80 Input Output Request
RD	Z-80 Read signal
INT	Z-80 Interrupt
CSCTC	Chip Select for the CTC
CSSIO	Chip Select for the SIO
MSEL4	Memory Select 4 for Sound Memory
CESM	Chip Enable Sound Memory
CSDISP	Chip Select for the Display
CSRADC	Chip Select Read Analog to Digital Convertor
SHSTB	Sample/Hold Strobe
CSWLVL	Chip Select Write Level Low
CSWPBL	Chip Write Push Button Latch
CSWLD0	Chip Select Write LED latch 0
SMA0	Sound Memory Address bit 0

SDB4 Sound Memory Data Bit 4

Since the schematics have so many pages, and there is not enough room to show all the interconnects, we have a separate list for interconnections. This list can be found following this document. It is arranged in alphabetical order. It shows the signal name, source page of signal, all destination pages and the full name of the signal.

NET LIST FOR SCHEMATIC SET FOR SP-12

SIGNAL NAME	SRC PG	DESTINATION PAGE	NOTES
+A0.D	1	2,3,4,6,8,16	Z-80 Addr. 0
+A1.D	1	2,3,4,6,8	Z-80 Addr. 1
+A2.D	1	3,4	Z-80 Addr. 2
+A3.D	1	3,4	Z-80 Addr. 3
+A4.D	1	3,4	Z-80 Addr. 4
+A5.D	1	3,4	" " 5
+A6.D	1	3,4	" " 6
+A7.D	1	3,4	" " 7
+A8.D	1	3,4	" " 8
+A9.D	1	3,4	" " 9
+A10.D	1	3,4	" " 10
+A11.D	1	3,4	" " 11
+A12.D	1	3,4	" " 12
+A13.D	1	3	" " 13
+A14.D	1	3	" " 14
+A15.D	1	3	" " 15
+ADCEOC	5	2	A/D End of Conversion
+C2MHZ	1	2	2 MHZ Clock
+C3MHZ	1	7,4	Microcontroller Clock
+C7.D	8	9	µC Carry Interconnect
+CARRY.D	9	7	µC Carry Out
-CESM.D	4	6	Sound Memory Chip Enable
-CLE.D	7	7,11-14	Carry Latch Enable
+CNL7.D	1	17	Channel 7 Clock for Sampling
+CNLS0.D	7	8,18	Channel Address 0 (These 3
+CNLS1.D	7	8,17	Channel Address 1 decode to
+CNLS2.D	7	8,17	Channel Address 2 0 thru 7)
-CNLS2.D	7	8	Channel Address 2 Inverted
+CNLSH0.V	18	19	Channel 0 Audio Sample and Hold
+CNLSH1.V	18	19	" 1 " "
+CNLSH2.V	18	19	" 2 " "
+CNLSH3.V	18	19	" 3 " "
+CNLSH4.V	18	19	" 4 " "
+CNLSH5.V	18	19	" 5 " "
+CNLSH6.V	18	19	" 6 " "
+CNLSH7.V	18	19	" 7 " "
-CSCTC	4	2	CTC Chip Select
+CSDSP.D	4	6	Display Chip Select
+CSRADC.D	4	5	Read ADC Chip Select
-CSRPB.D	4	5	Read Pushbuttons Chip Select

NET LIST FOR SCHEMATIC SET FOR SP-12

SIGNAL NAME	SRC PG	DESTINATION PAGE	NOTES
-CSSIO.D	4	2	SIO Chip Select
-CSSM.D	4	16	Sound RAM Chip Select
+CSWADC.D	4	5	Write ADC Chip Select
-CSWAD	4	7	Z-80 Write Reg. File Addr. CS
-CSWHI	4	7	Z-80 to uC Write Hi Byte CS
-CSWLD0.D	4	6	Write LED Latch 0 CS
-CSWLD1.D	4	6	" " " 1 "
-CSWLO.D	4	9	Z-80 to µC Write Lo Byte CS
-CSWLVH.D	4	8	Write Loudness Volume High CS
-CSWLVL.D	4	8	" " " Low "
-CSWPBL.D	4	5	Write Pushbuttons Latch CS
+D0.D	1	2,3,4,5,6,7,8,9,16	Z-80 Data Buss Bit 0
+D1.D	1	2,3,4,5,6,7,8,9,16	" " " " 1
+D2.D	1	2,3,4,5,6,7,8,9,16	" " " " 2
+D3.D	1	2,3,4,5,6,7,8,9,16	" " " " 3
+D4.D	1	2,3,4,5,6,7,8,9,16	" " " " 4
+D5.D	1	2,3,4,5,6,7,8,9,16	" " " " 5
+D6.D	1	2,3,4,5,6,7,8,9,16	" " " " 6
+D7.D	1	2,3,4,5,6,7,8,9,16	" " " " 7
+DACOUT.V	18	17	Pre Demultiplexed Audio
-DOE.D	7	9	µC Data Latch Output Enable
+GAIN1.D	5	6	Sample Gain Range 1Select
-GAIN2.D	5	6	Sample Gain Range 2 Select
+IL7.D	8	9	Increment Latch Bit 7
-ILE.D	7	8	Increment Latch Enable
-INPUT.D	5	16,17	Sample Data Latch Output Enable
-INT.D	2	1	Z-80 Interrupt
-IORQ.D	1	2,4,16	Z-80 I/O Request
+LD0.D	8	18	Level Data Bit 0
+LD1.D	8	18	Level Data Bit 1
+LD2.D	8	18	" " " 2
+LD3.D	8	18	" " " 3
+LD4.D	8	18	" " " 4
+LD5.D	8	18	" " " 5
+LD6.D	8	18	" " " 6
+LD7.D	8	18	" " " 7
-M1.D	1	2	Z-80 M1
-MLE.D	7	7,9	Sound Memory Addr. Latch Enable
-MREQ.D	1	3	Z-80 Memory Request
-MSEL4.D	3	4	Z-80 RAM Memory Select 4

NET LIST FOR SCHEMATIC SET FOR SP-12

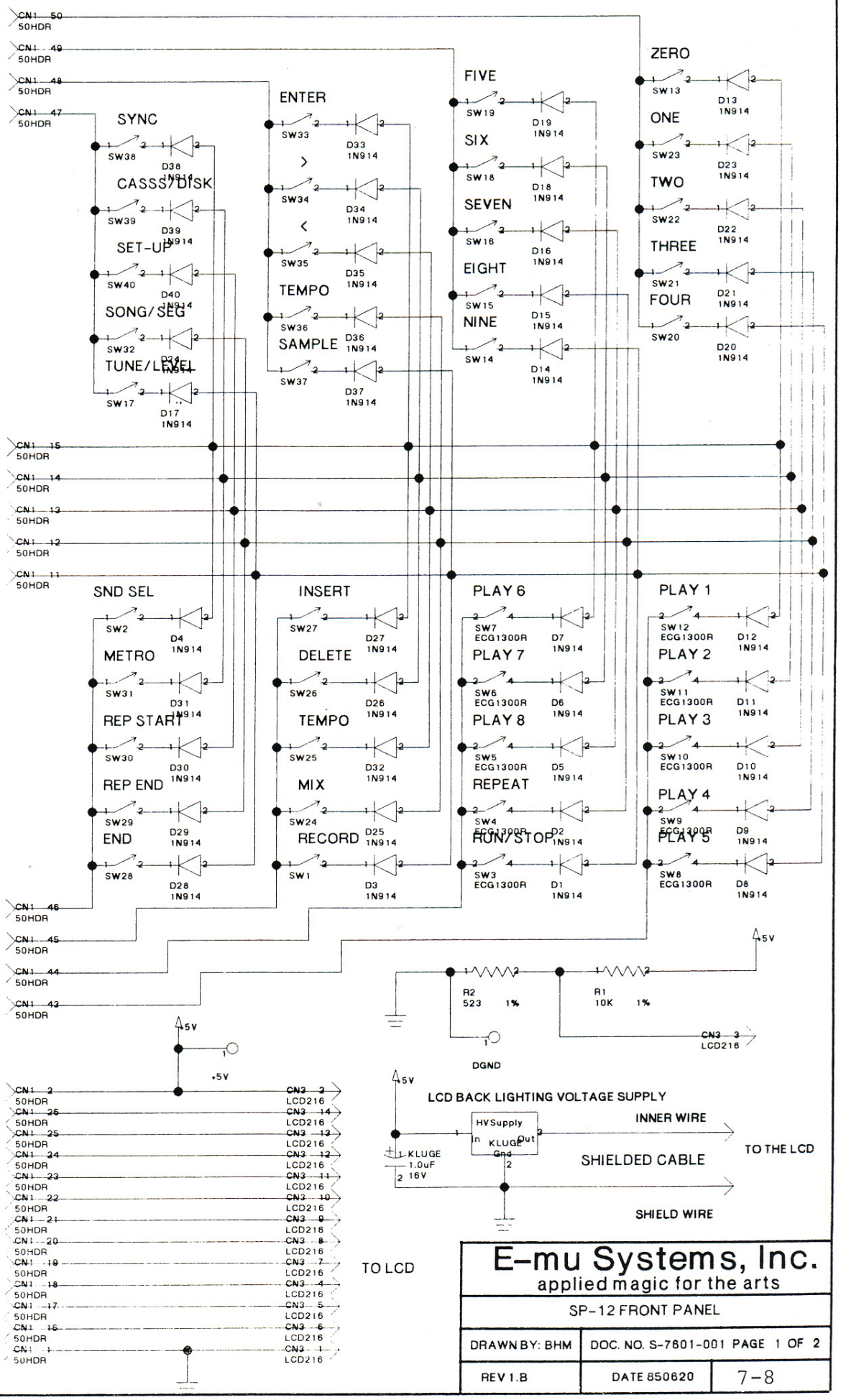
SIGNAL NAME	SRC PG	DESTINATION PAGE	NOTES
-MSEL5.D	3	4	" " " " 5
-MSEL6.D	3	4	" " " " 6
-MSEL7.D	3	4	" " " " 7
-NMI.D	1	6	Z-80 Non-Maskable Interrupt
+PHI.D	1	2	Z-80 Clock
+PWROK.D	20	1,3,4,10	DC Power OK Signal
+RA0.D	7	8,9	Register File Address Bit 0
+RA1.D	7	8,9	" " " " 1
+RA2.D	7	8,9	" " " " 2
+RA3.D	7	8,9	" " " " 3
+RA4.D	7	8,9	" " " " 4
+RA5.D	7	8,9	" " " " 5
+RA6.D	7	8,9	" " " " 6
+RA7.D	7	8,9	" " " " 7
+RDB16.D	9	8	Register File Data Bit 16
+RDB17.D	9	8	" " " " 17
+RDB18.D	9	8	" " " " 18
+RDB19.D	9	8	" " " " 19
+RDB20.D	9	8	" " " " 20
+RDB21.D	9	8	" " " " 21
+RDB22.D	9	8	" " " " 22
+RDB23.D	9	8	" " " " 23
-RD.D	1	2,3,4	Z-80 Read
-RESET.D	1	2	Reset
-RSTPB.D	6	20	Force Reset Test Point
-RWP.D	7	8,9	Register File Read/Write
+SDB0.D	16	18	Sound Data Bit 0 (Demux'd
+SDB1.D	16	18	" " " 1 A +B Buss)
+SDB2.D	16	18	" " " 2
+SDB3.D	16	18	" " " 3
+SDB0A.D	10-14,17	16	Sound Data Buss A Bit 0
+SDB1A.D	10-14,17	16	" " " " " 1
+SDB2A.D	10-14,17	16	" " " " " 2
+SDB3A.D	10-14,17	16	" " " " " 3
+SDB0B.D	10-14,17	16	Sound Data Buss B Bit 0
+SDB1B.D	10-14,17	16	" " " " " 1
+SDB2B.D	10-14,17	16	" " " " " 2
+SDB3B.D	10-14,17	16	" " " " " 3
+SDB4.D	10-14,17	16	Sound Data Buss Bit 4
+SDB5.D	10-14,17	16	" " " " 5

NET LIST FOR SCHEMATIC SET FOR SP-12

SIGNAL NAME	SRC PG	DESTINATION PAGE	NOTES
+SDB6.D	10-14,17	16	" " " " 6
+SDB7.D	10-14,17	16	" " " " 7
+SDB8.D	10-14,17	16	" " " " 8
+SDB9.D	10-14,17	16	" " " " 9
+SDB10.D	10-14,17	16	" " " " 10
+SDB11.D	10-14,17	16	" " " " 11
+SHSTB.D	4	18	Sample Hold Strobe
+SIOEO.D	2	2	SIO Interrupt Enable Out
+SMA0.D	9	10-14	Sound Memory Address Bit 0
+SMA1.D	9	10-14	" " " " 1
+SMA2.D	9	10-14	" " " " 2
+SMA3.D	9	10-14	" " " " 3
+SMA4.D	9	10-14	" " " " 4
+SMA5.D	9	10-14	" " " " 5
+SMA6.D	9	10-14	" " " " 6
+SMA7.D	9	10-14	" " " " 7
+SMA8.D	9	10-14	" " " " 8
+SMA9.D	9	10-14	" " " " 9
+SMA10.D	9	10-14	" " " " 10
+SMA11.D	9	10-14	" " " " 11
+SAM12.D	9	10-14	" " " " 12
+SMA13.D	9	10-14	" " " " 13
-SMA13.D	11	12-14	RAM Sound Memory Chip Select
+SMA14.D	9	10,11,13	Sound Memory Address Bit 14
+SMA15.D	9	10,11,13	" " " " 15
+SMA16.D	8	10	" " " " 16
+SMA17.D	8	10	" " " " 17
+SMA18.D	8	10	" " " " 18
-SMCS2.D	10	15	RAM Sound Memory Chip Select
-SMCS3.D	10	15	" " " " "
-SMCS4.D	10	15	" " " " "
-SMCS5.D	10	15	" " " " "
-SMCS6.D	10	13	" " " " "
-SMCS62.D	13	14	" " " " "
-SMCS63.D	13	14	" " " " "
-SMCS7.D	10	11	" " " " "
-SMCS72.D	11	12	" " " " "
-SMCS73.D	11	12	" " " " "
-SMOE.D	16	10-15	Sound Memory Output Enable
-SWEH.D	16	11-15	Sound Mem. Write Enable High

NET LIST FOR SCHEMATIC SET FOR SP-12

SIGNAL NAME	SRC PG	DESTINATION PAGE	NOTES
-SWEL.D	16	11-15	" " " " " " Low
-TOE.D	7	8,9	Temporary Latch Output Enable
+UCK.D	7	7,8,9	µC Main Clock
-UCK.D	1	4,7,16	µC Main Clock Inverted
+UCNL0.D	1	7,16	µC Channel Address 0
+UCNL1.D	1	7,16	µC Channel Address 1
+UCNL2.D	1	7,16	µC Channel Address 2
+UCNT0.D	1	4,7,16	µC State Counter Bit 0
+UCNT1.D	1	4,7,16	" " " " 1
+UCNT2.D	1	4,7,16	" " " " 2
-WAIT.D	16	1	Z-80 Wait
-WR.D	1	3,4,16	Z-80 Write



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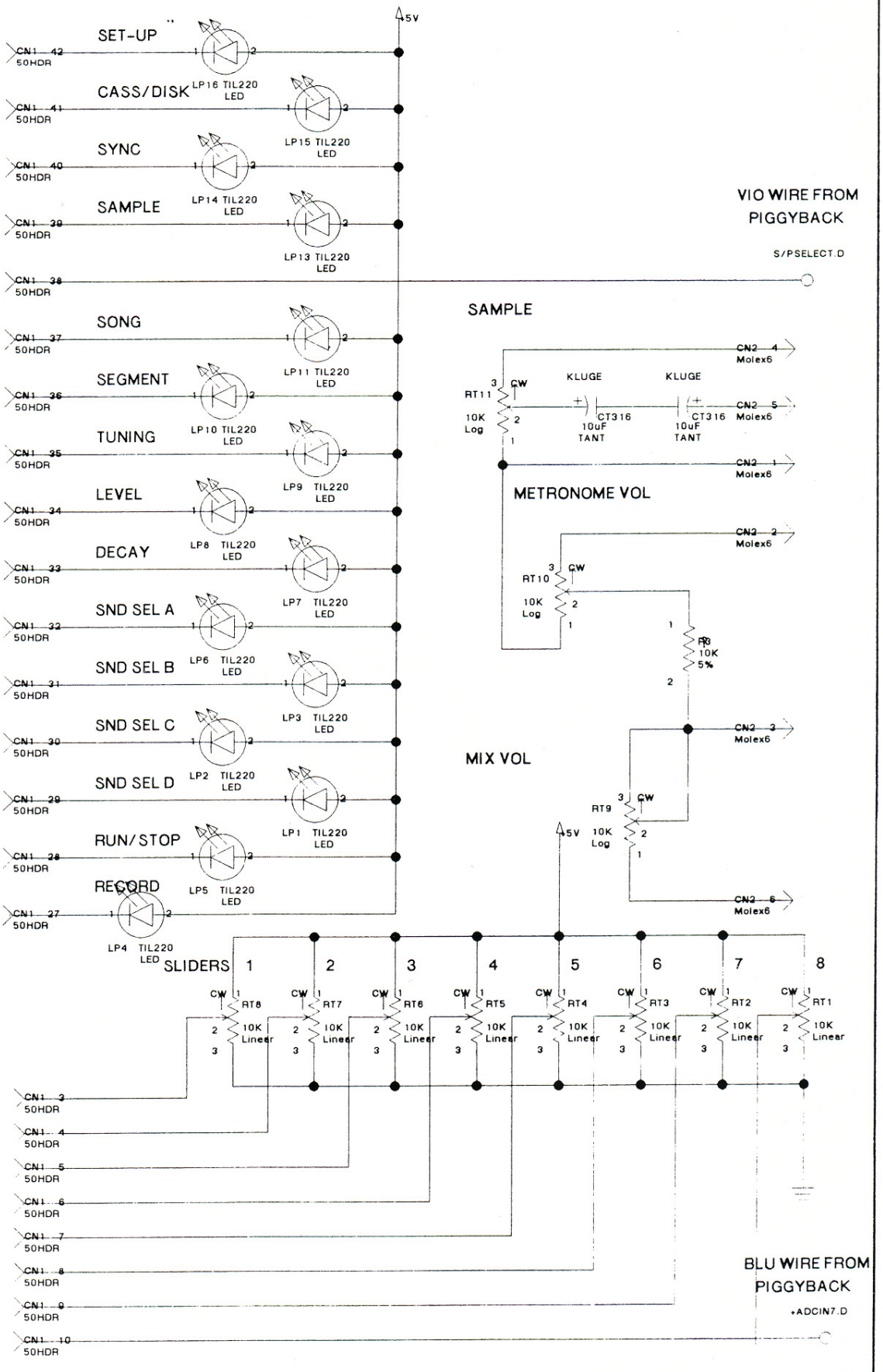
SP-12 FRONT PANEL

DRAWN BY: BHM	DOC. NO. S-7601-001 PAGE 1 OF 2	
REV 1.B	DATE 850620	7-8



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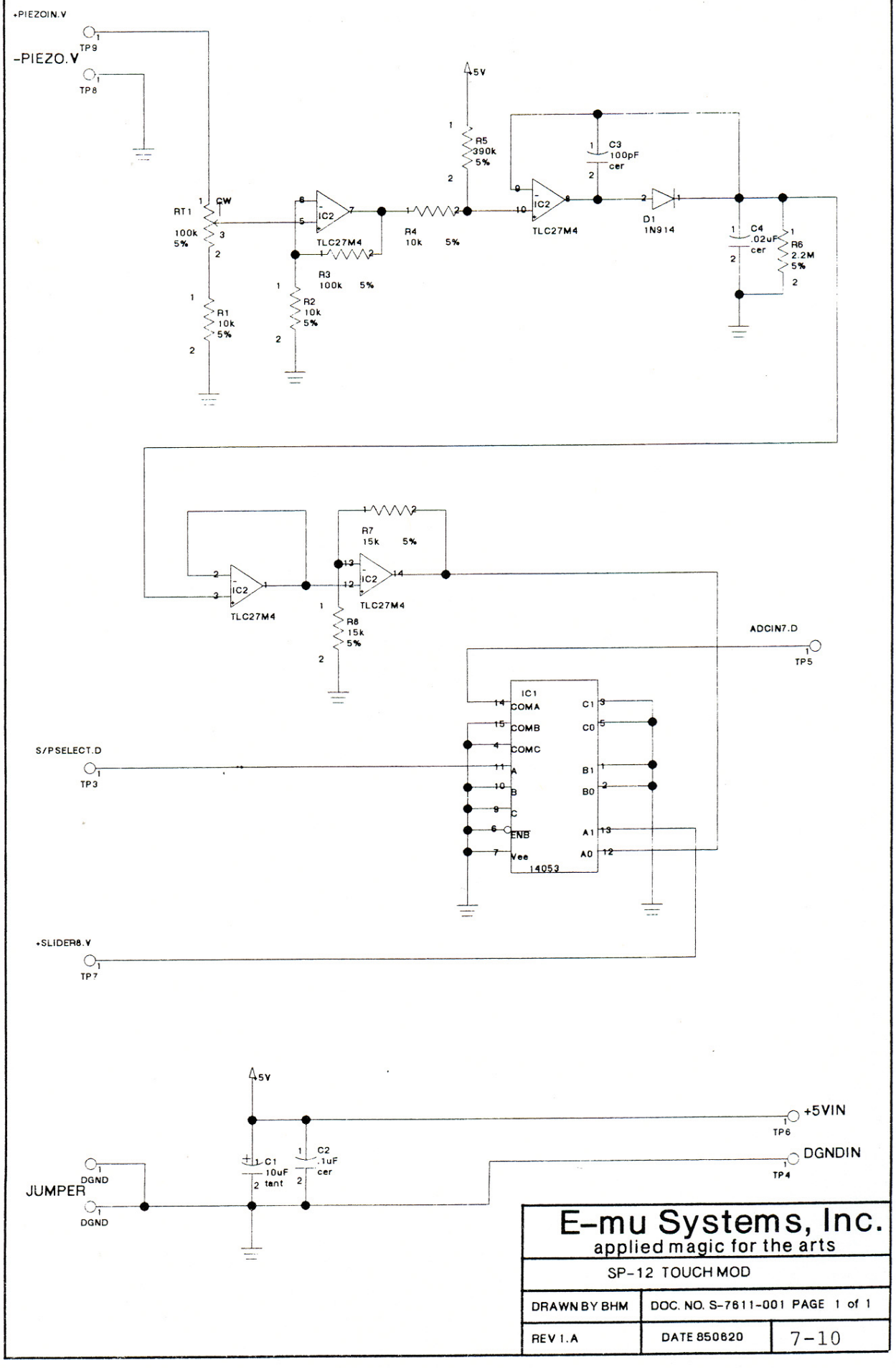
SP-12 FRONT PANEL	
DOC. NO. S-7601-001 PAGE 2 OF 2	7-9



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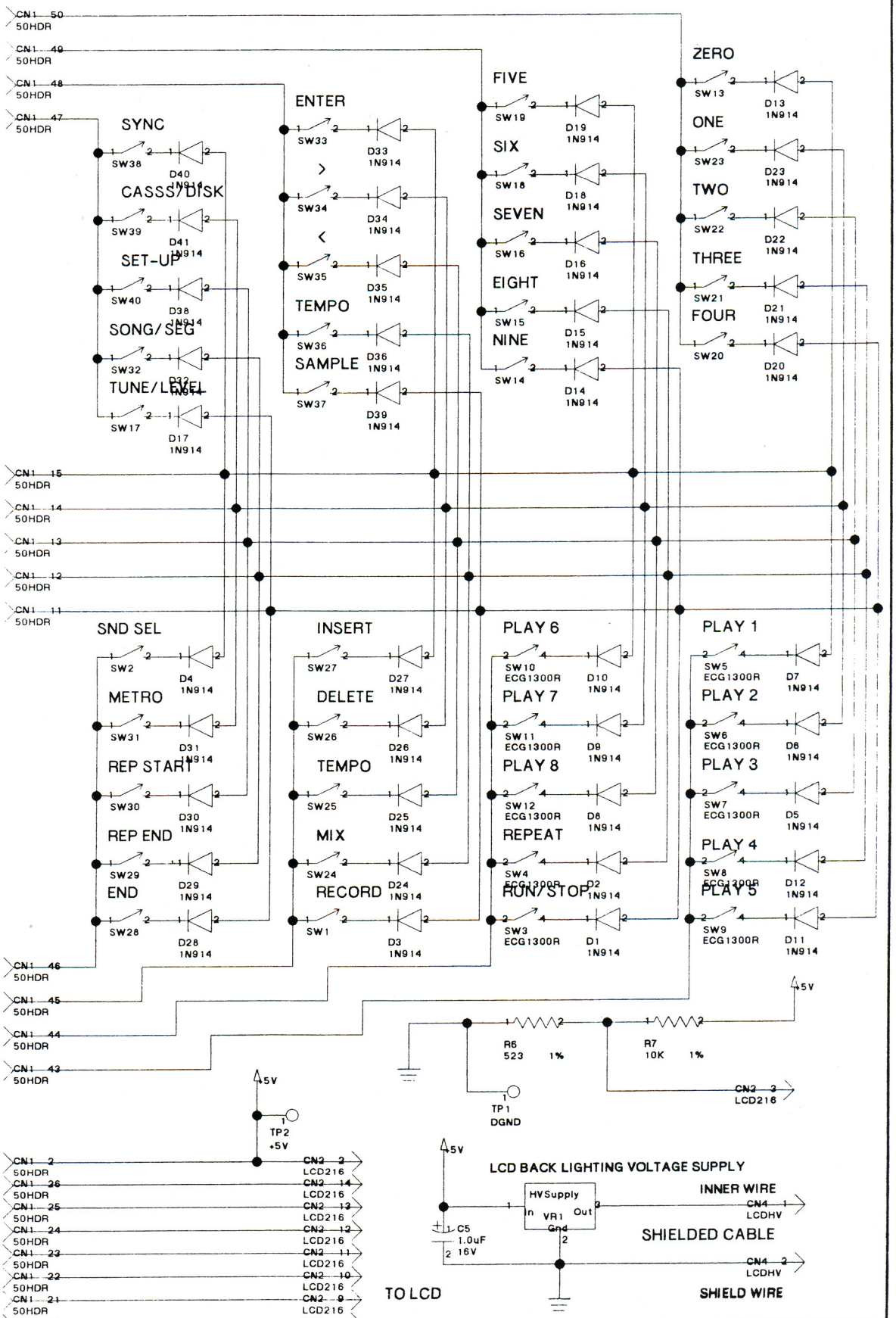
SP-12 TOUCH MOD		
DRAWN BY BHM	DOC. NO. S-7611-001 PAGE 1 of 1	
REV 1.A	DATE 850620	7-10



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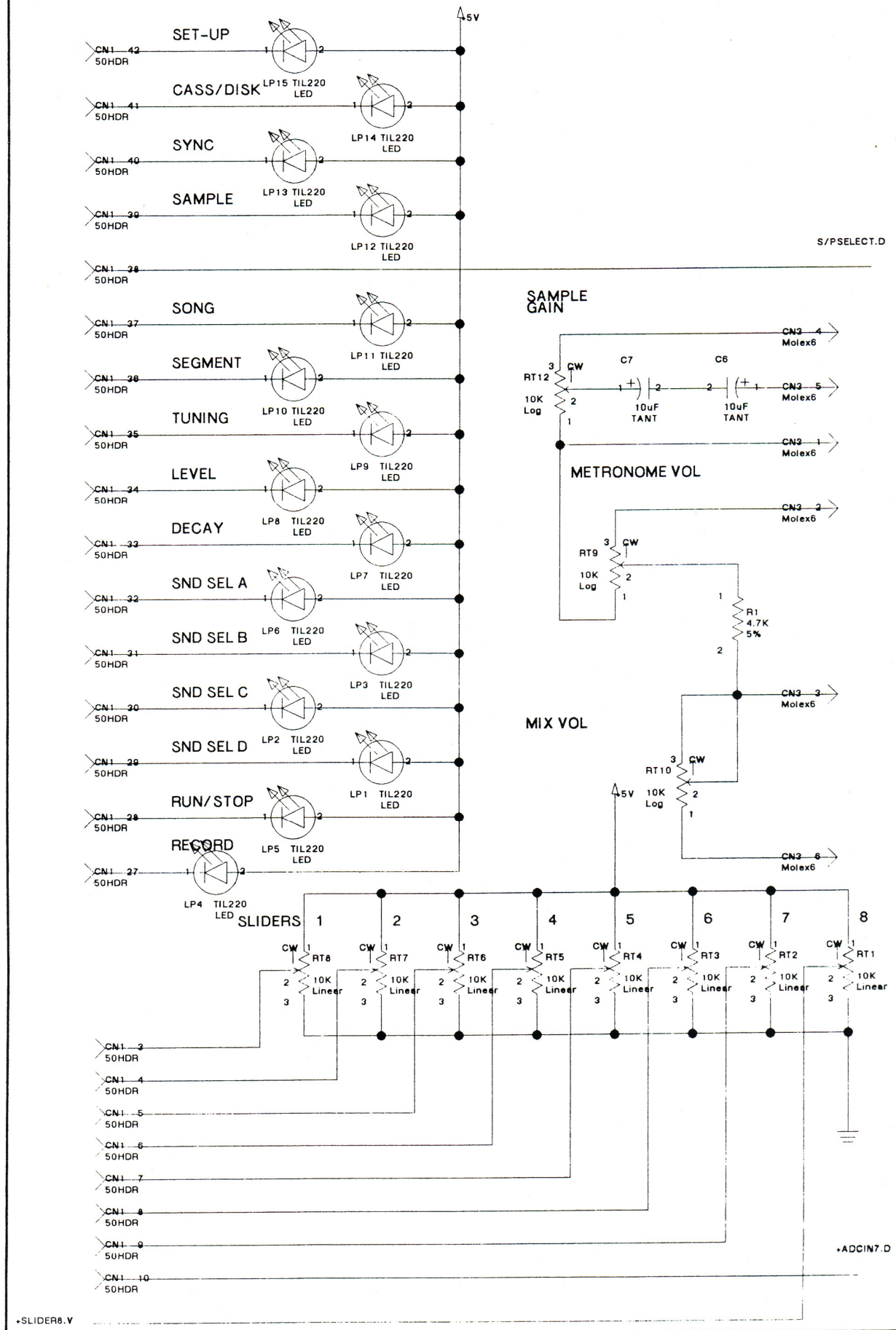
SP-12 FRONT PANEL

DRAWN BY: BHM	DOC. NO. S-7601-001 PAGE 1 OF 4	
REV 2.A	DATE 850703	7-11



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SP-12 FRONT PANEL	
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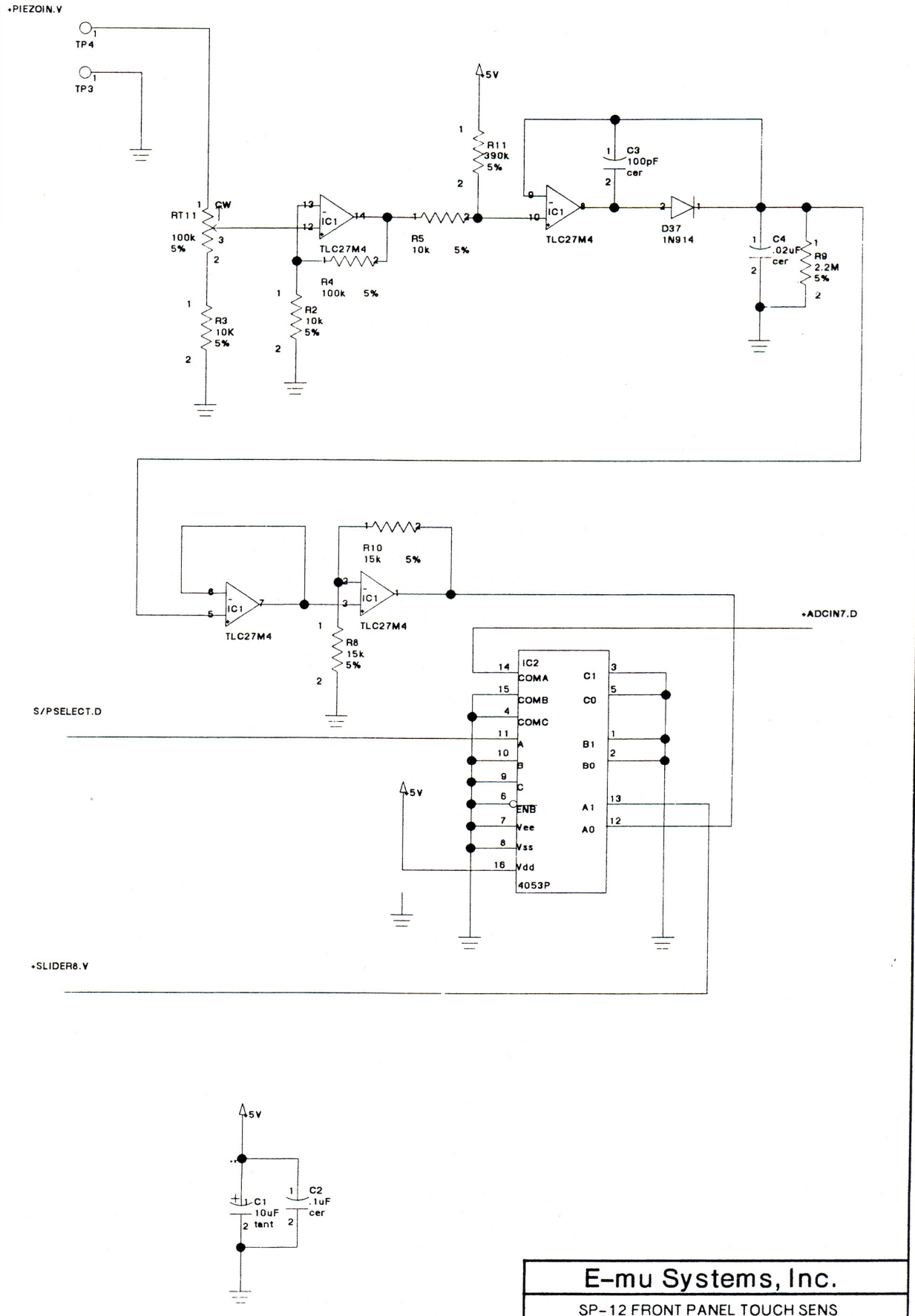

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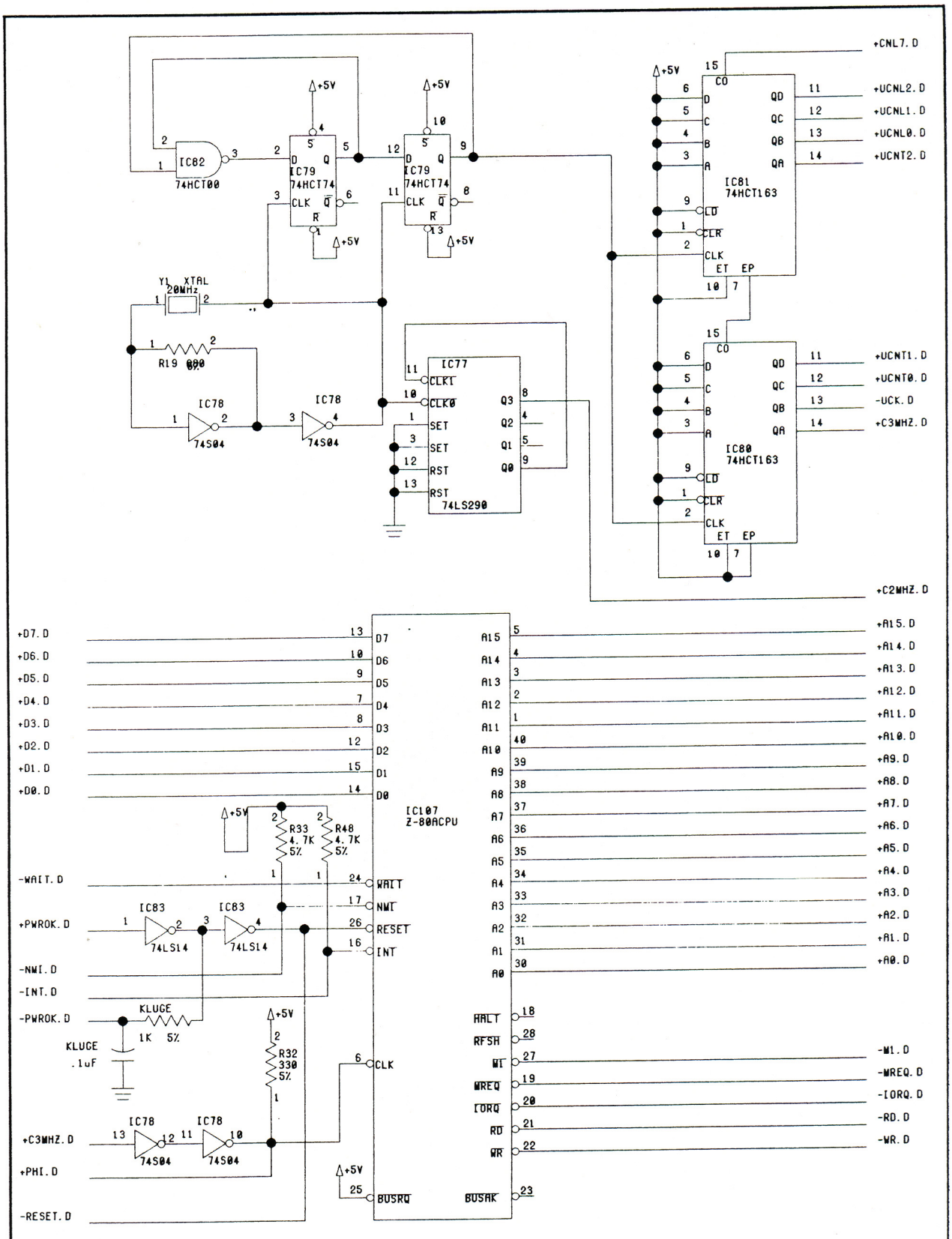
RIBBON CABLE CONNECTIONS

CN1 OF THE MAIN PWA		CN1 OF THE FRONT PANEL PWA
PIN #	SIGNAL NAME OR SOURCE/DESTINATION	PIN #
1	IC11 PIN 9	50
2	IC11 PIN 7	49
3	IC11 PIN6	48
4	IC11 PIN 5	47
5	IC11 PIN4	46
6	IC11 PIN3	45
7	IC11 PIN2	44
8	IC11 PIN1	43
9	IC30 PIN19	42
10	IC30 PIN16	41
11	IC30 PIN15	40
12	IC30 PIN12	39
13	IC30 PIN9	38
14	IC30 PIN6	37
15	IC30 PIN5	36
16	IC30 PIN2	35
17	IC29 PIN19	34
18	IC29 PIN 16	33
19	IC29 PIN15	32
20	IC29 PIN12	31
21	IC29 PIN9	30
22	IC29 PIN6	29
23	IC29 PIN5	28
24	IC29 PIN2	27
25	+D7.D	26
26	+D6.D	25
27	+D5.D	24
28	+D4.D	23
29	+D3.D	22
30	+D2.D	21
31	+D1.D	20
32	+D0.D	19
33	+A0.D	18
34	+A1.D	17
35	+CSDISP.D	16
36	IC39 PIN8	15
37	IC39 PIN6	14
38	IC39 PIN4	13
39	IC39 PIN2	12
40	IC39 PIN11	11
41	IC40 PIN5	10
42	IC40 PIN4	9
43	IC40 PIN3	8
44	IC40 PIN2	7
45	IC40 PIN1	6
46	IC40 PIN28	5
47	IC40 PIN27	4
48	IC40 PIN26	3
49	+5V	2
50	DGND	1



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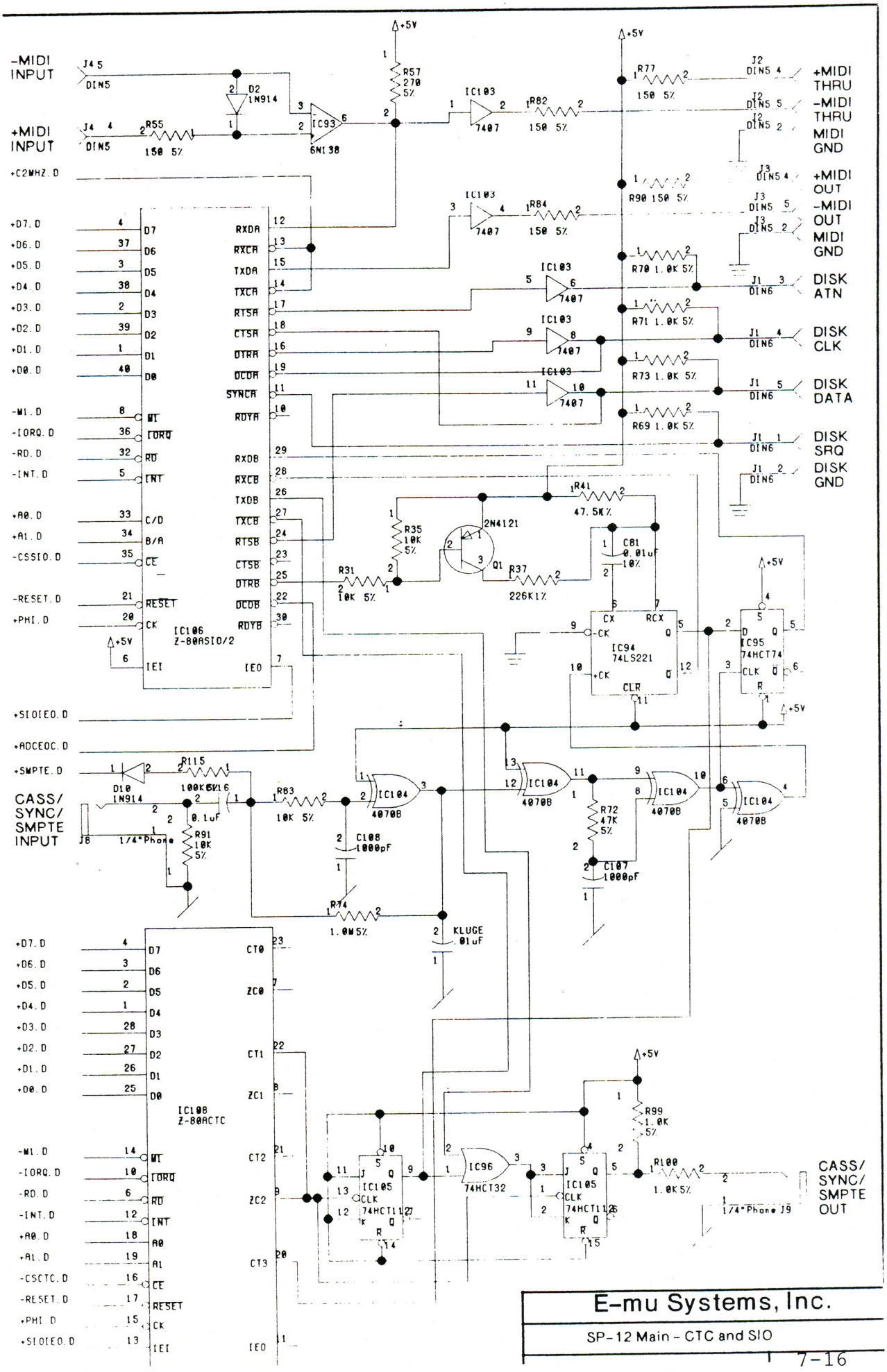
SP-12 Main - Clocks and CPU

DRAWN BY: DPR	DOC. NO. S-7600-001 PAGE 1 OF 21	
REV 1.N	DATE 851218	7-15



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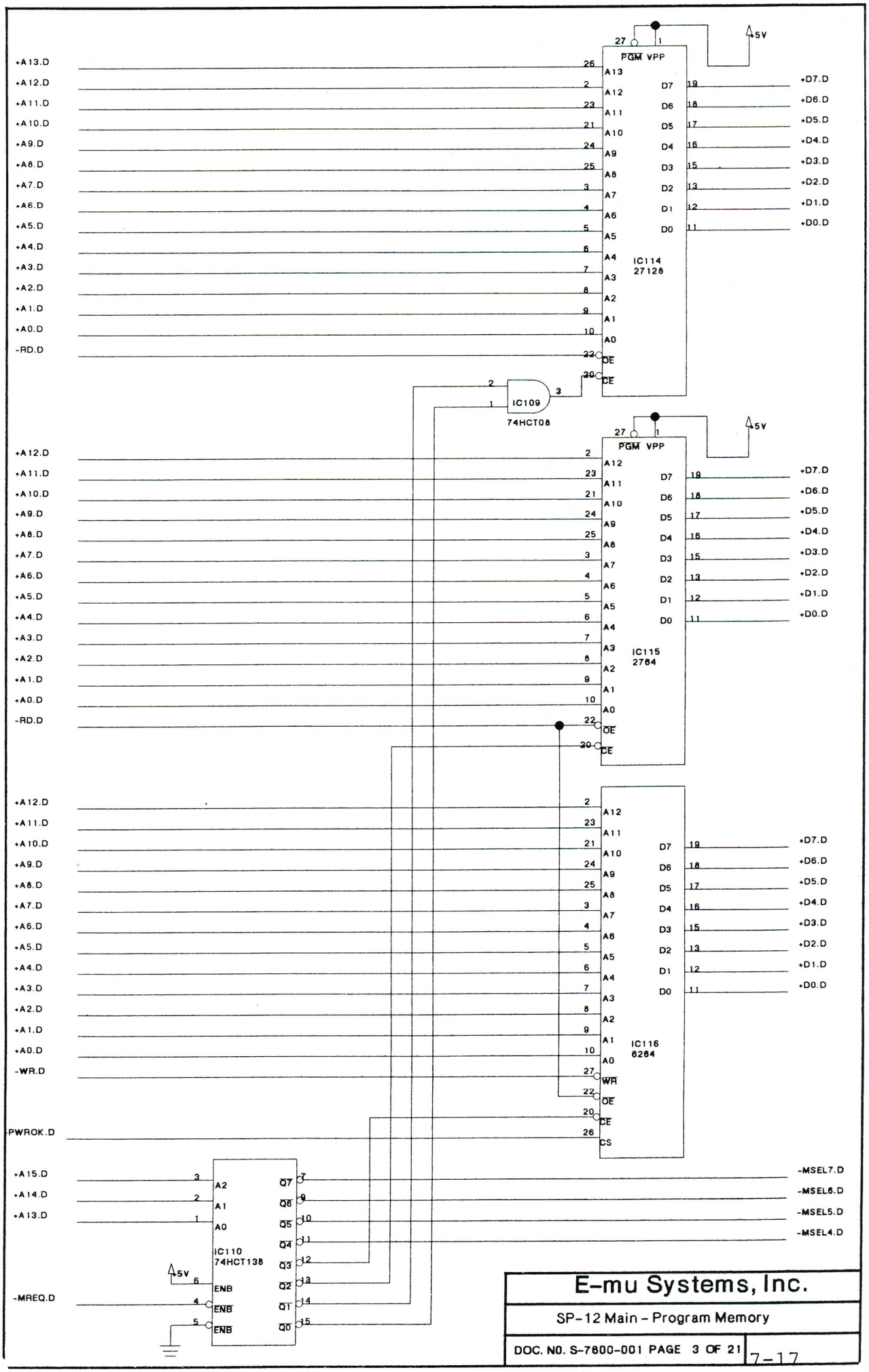
SP-12 Main - CTC and SIO


+A13.D
+A12.D
+A11.D
+A10.D
+A9.D
+A8.D
+A7.D
+A6.D
+A5.D
+A4.D
+A3.D
+A2.D
+A1.D
+A0.D
-RD.D
27
1
5V
PGM VPP
26
A13
2
A12
23
A11
21
A10
24
A9
25
A8
3
A7
4
A6
5
A5
6
A4
7
A3
8
A2
9
A1
10
A0
22
OE
20
CE
D7
D6
D5
D4
D3
D2
D1
D0
19
18
17
16
15
13
12
11
+D7.D
+D6.D
+D5.D
+D4.D
+D3.D
+D2.D
+D1.D
+D0.D
IC114
27128
2
1
IC109
74HCT08
3
+A12.D
+A11.D
+A10.D
+A9.D
+A8.D
+A7.D
+A6.D
+A5.D
+A4.D
+A3.D
+A2.D
+A1.D
+A0.D
-RD.D
IC115
2764
+A12.D
+A11.D
+A10.D
+A9.D
+A8.D
+A7.D
+A6.D
+A5.D
+A4.D
+A3.D
+A2.D
+A1.D
+A0.D
-WR.D
WR
IC116
6264
-PWROK.D
CS
+A15.D
+A14.D
+A13.D
A2
A1
A0
IC110
74HCT138
5V
-MREQ.D
ENB
ENB
ENB
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
7
9
10
11
12
13
14
15
-MSEL7.D
-MSEL6.D
-MSEL5.D
-MSEL4.D
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SP-12 Main - Program Memory
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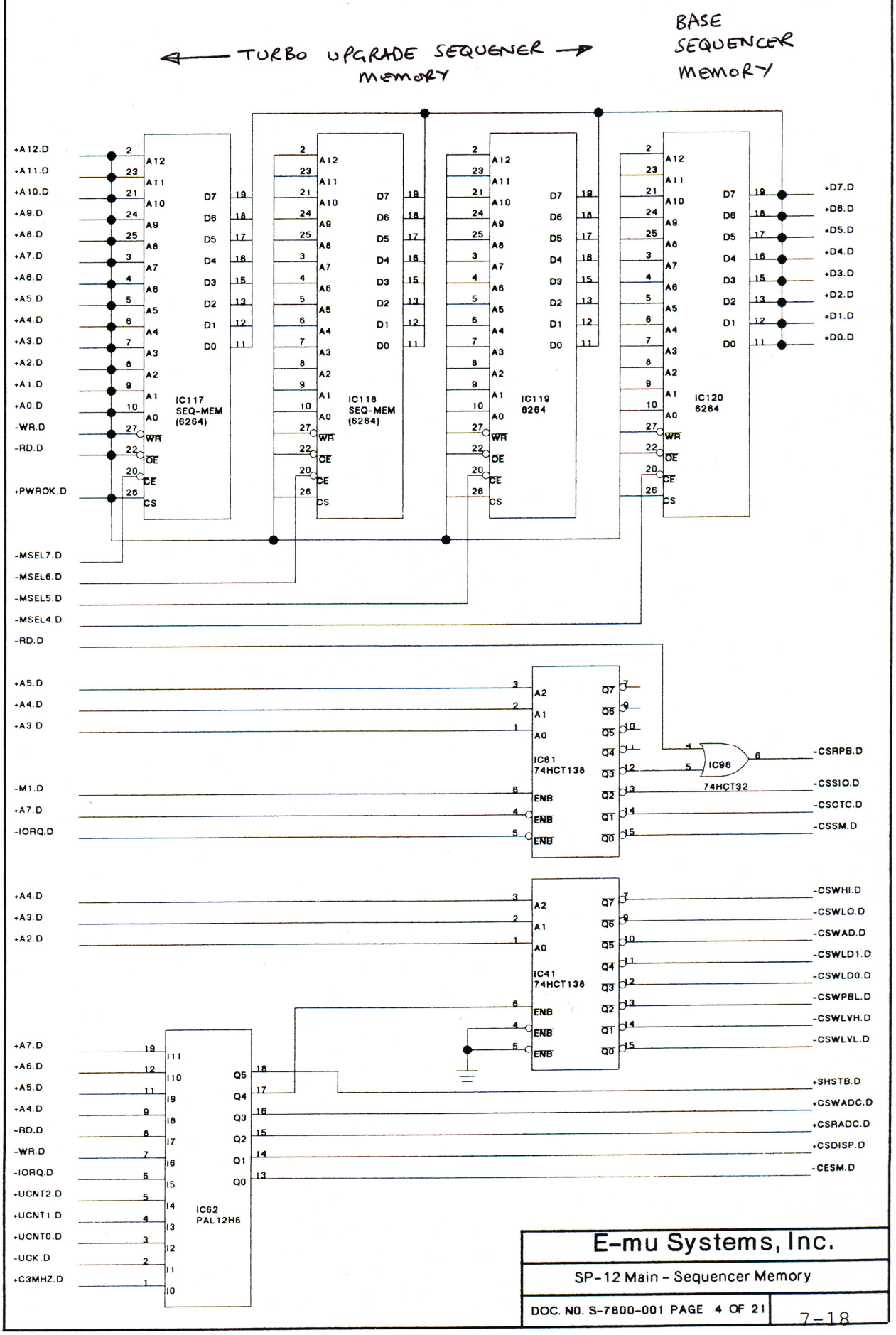

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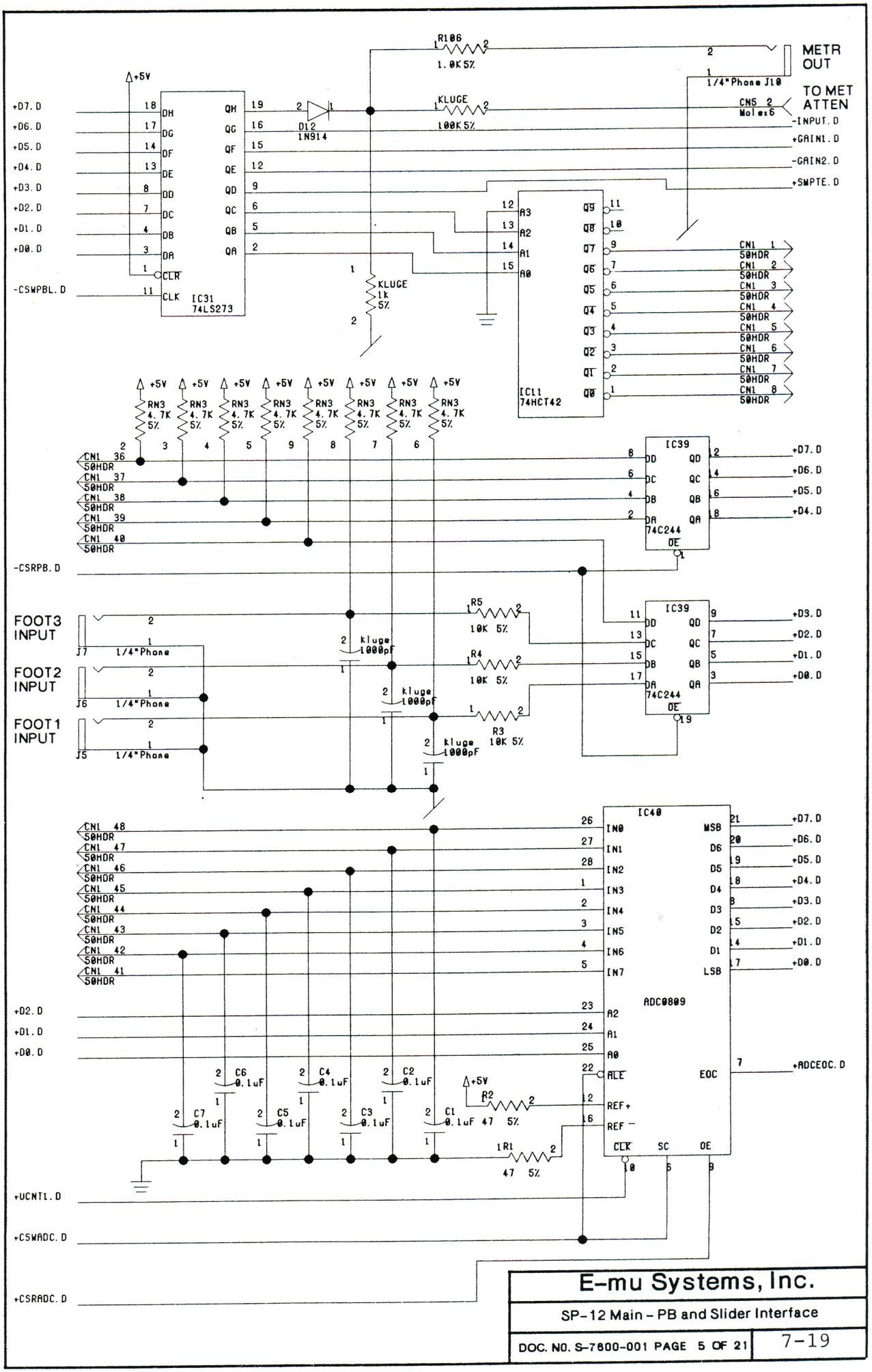
SP-12 Main - Sequencer Memory	
DOC. NO. S-7800-001 PAGE 4 OF 21	7-18



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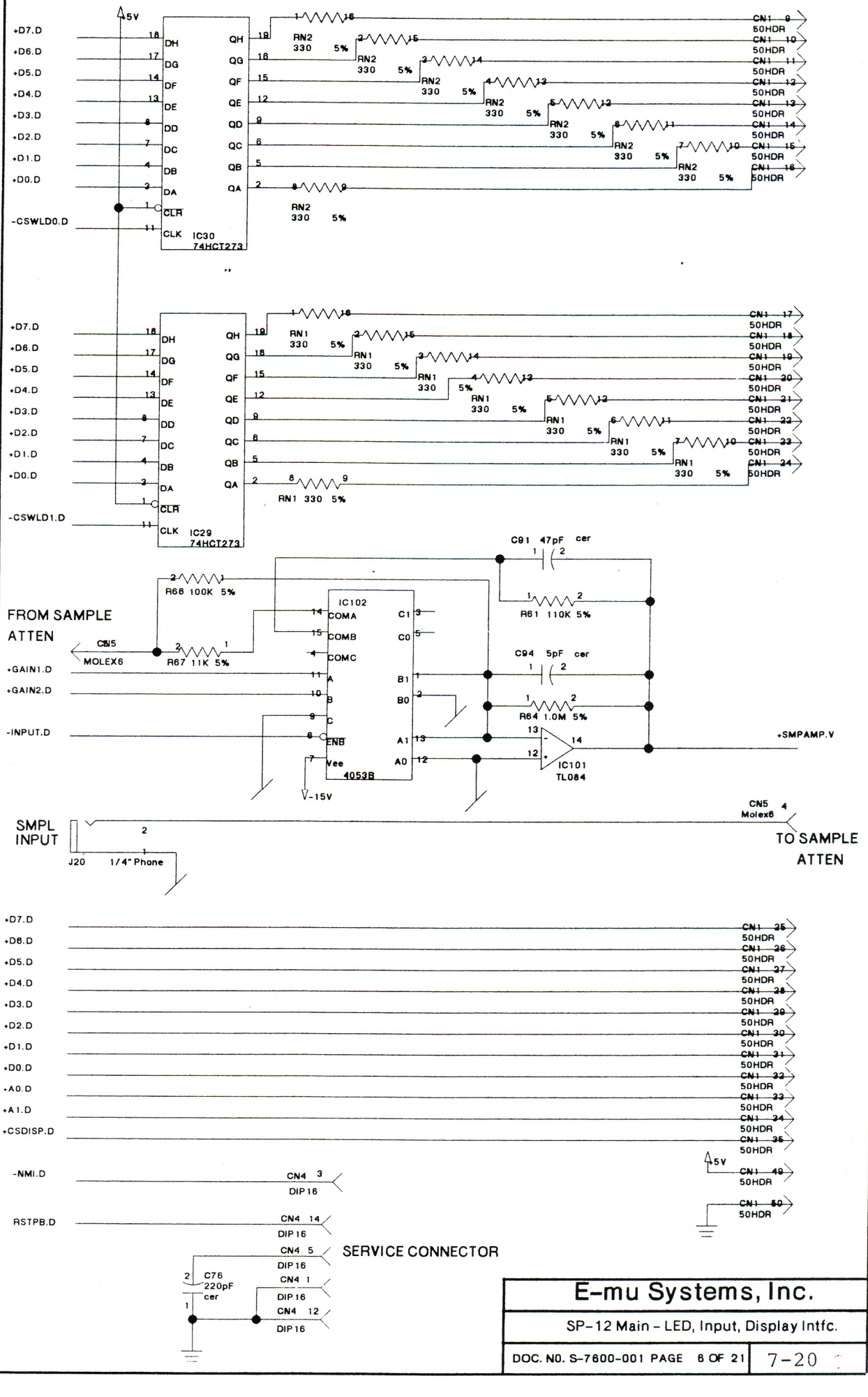
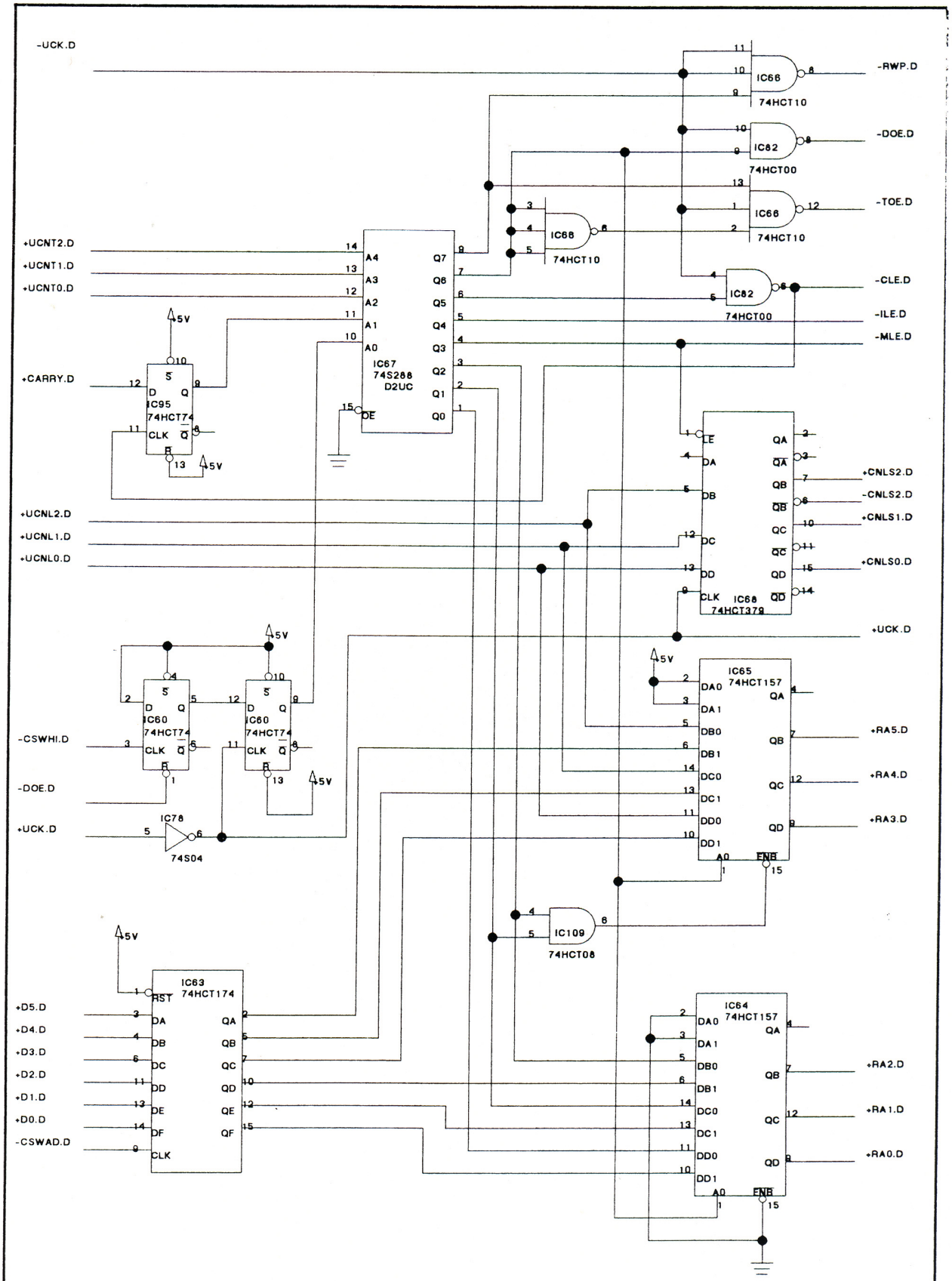
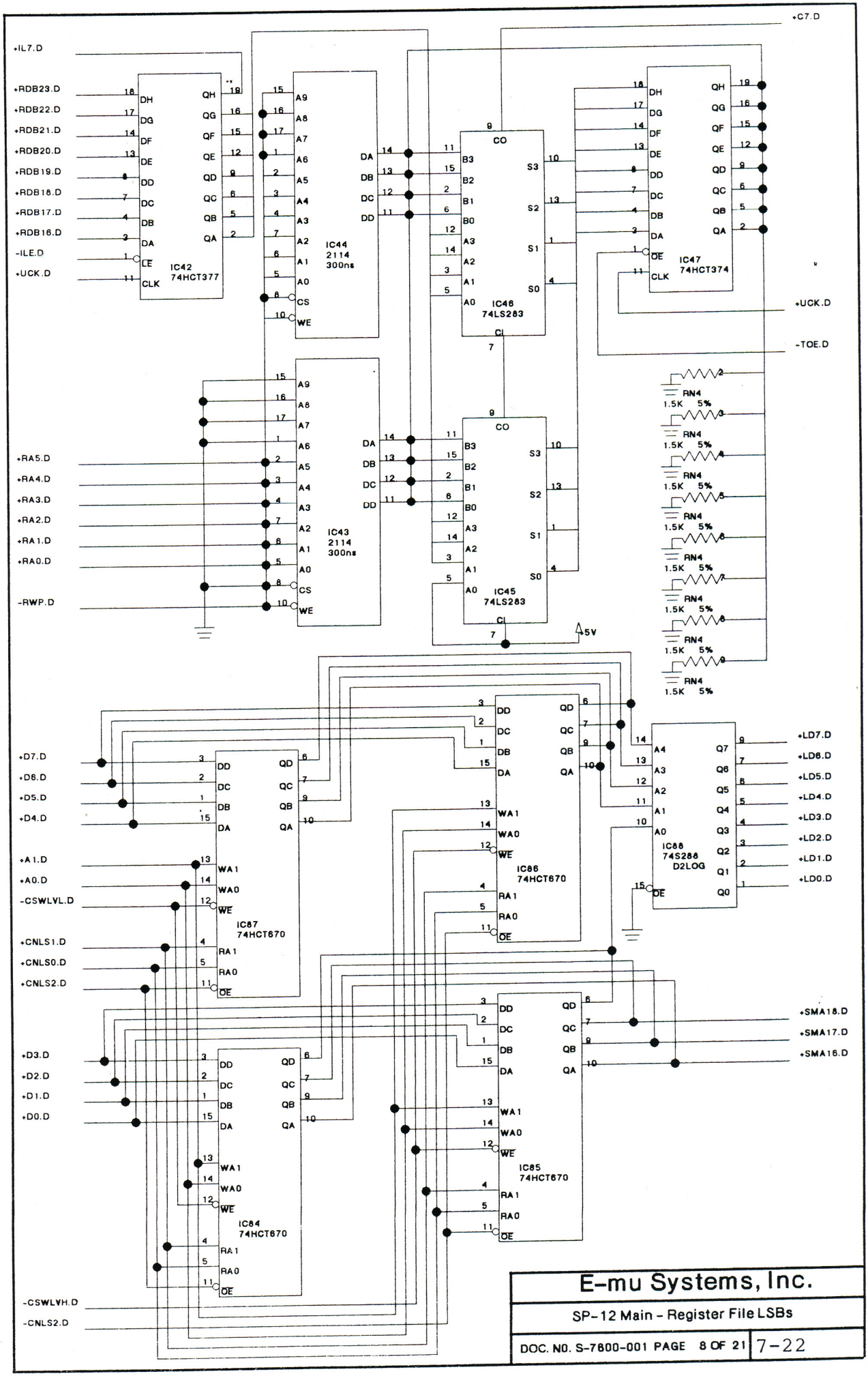
SP-12 Main - PB and Slider Interface	
DOC. NO. S-7800-001 PAGE 5 OF 21	7-19



E-mu Systems, Inc.	
SP-12 Main - LED, Input, Display Intfc.	
DOC. NO. S-7600-001 PAGE 8 OF 21	7-20

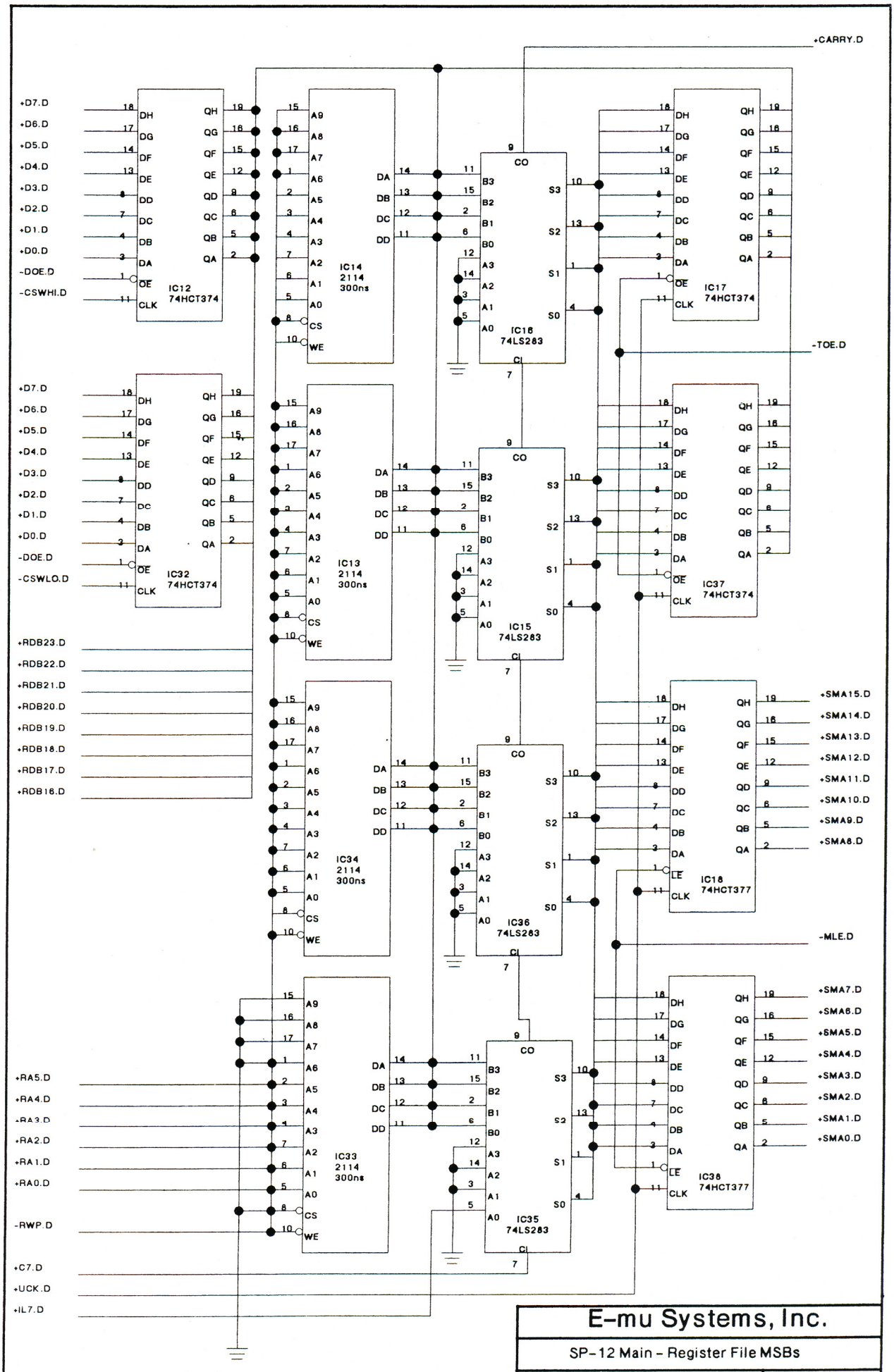


E-mu Systems, Inc.	
SP-12 Main - Control Sequencer	
DOC. NO. S-7800-001 PAGE 7 OF 21	7-21

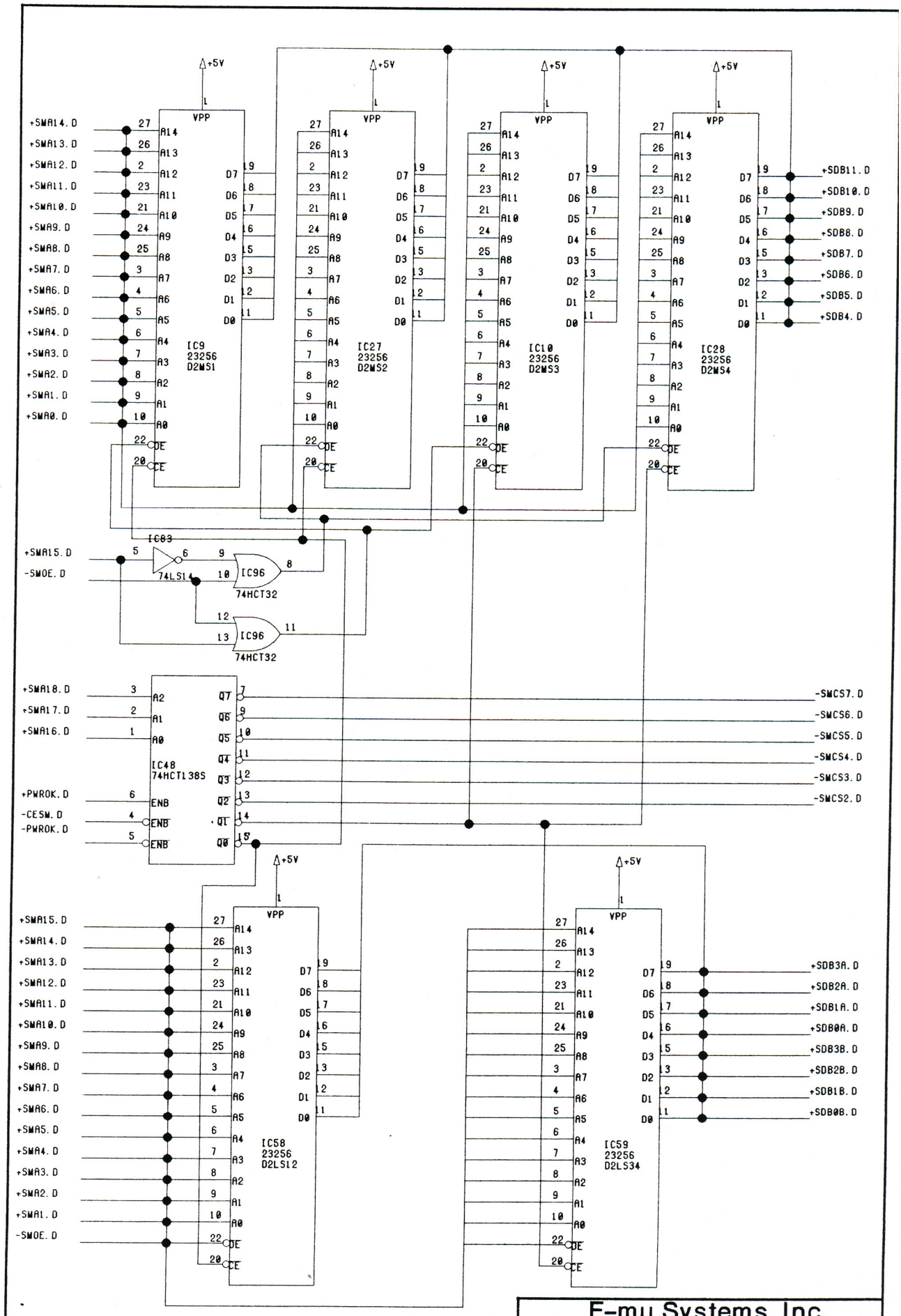


E-mu Systems, Inc.

SP-12 Main - Register File LSBs



E-mu Systems, Inc.	
SP-12 Main - Register File MSBs	
DOC. NO. S-7600-001 PAGE 9 OF 21	7-23



E-mu Systems, Inc.

SP-12 Main - ROM Sound Memory

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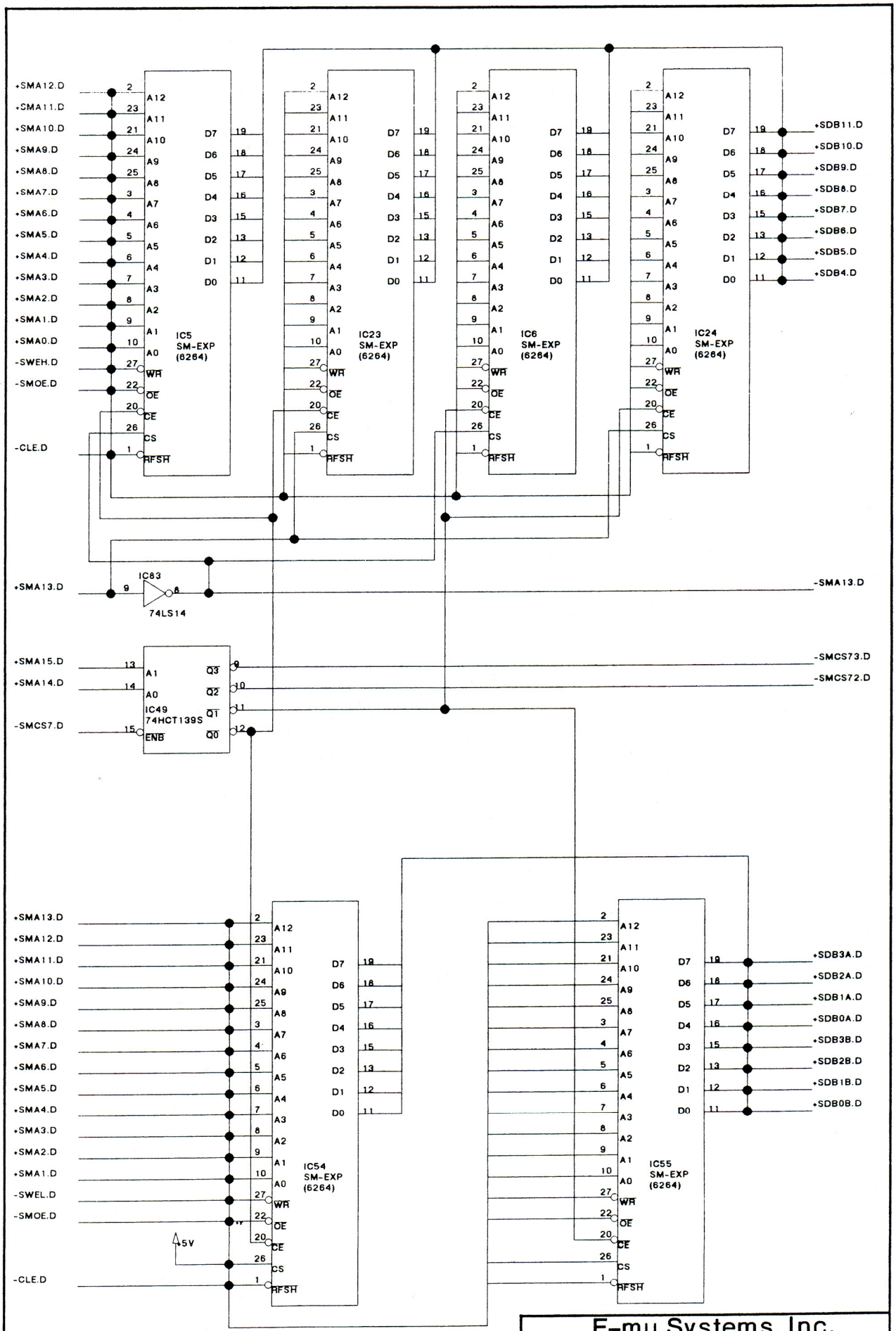
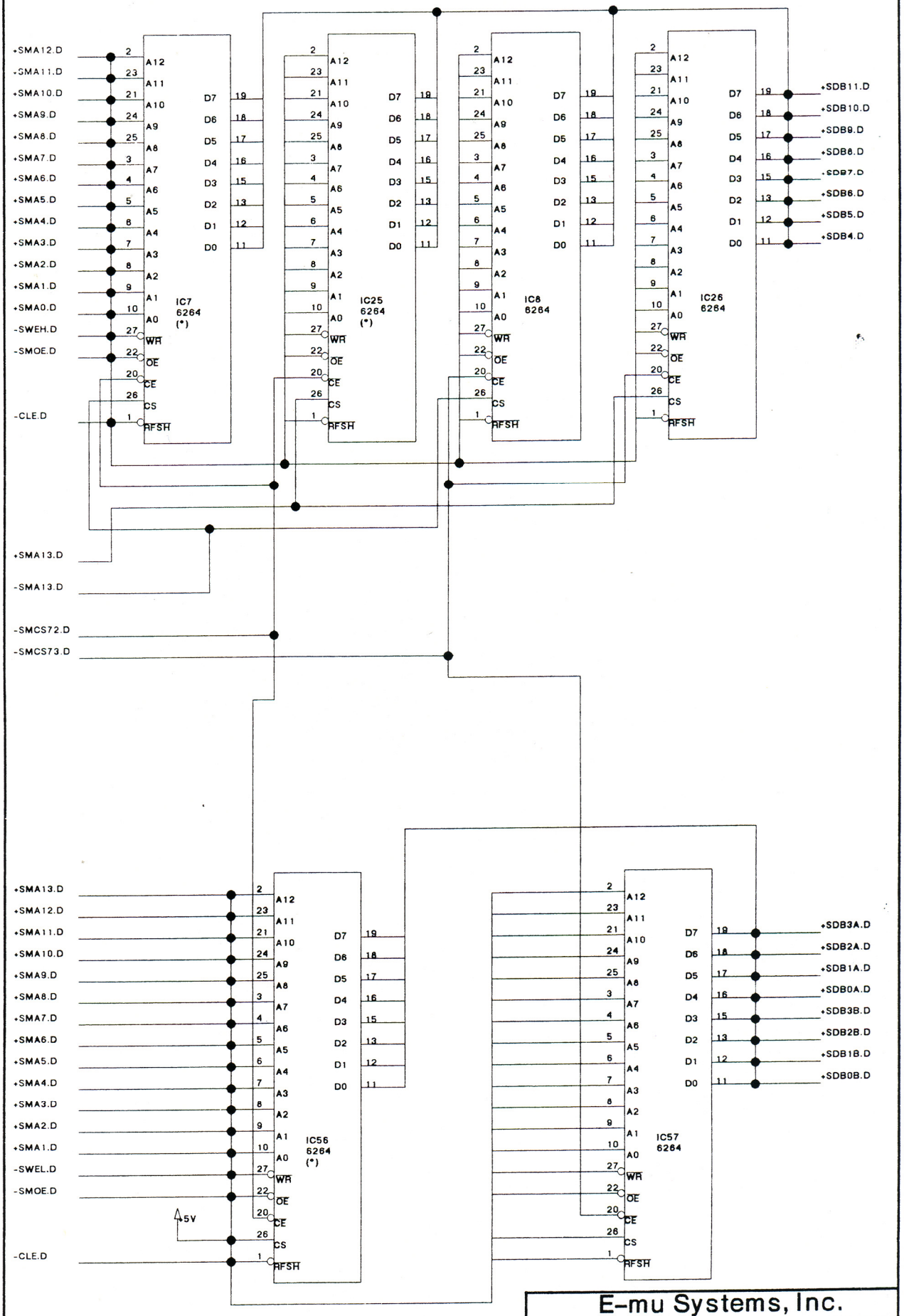


E-mu Systems, Inc.

SP-12 Main - RAM Sound Memory

DOC. NO. S-7600-001 PAGE 11 OF 21



E-mu Systems, Inc.

SP-12 Main - RAM Sound Memory

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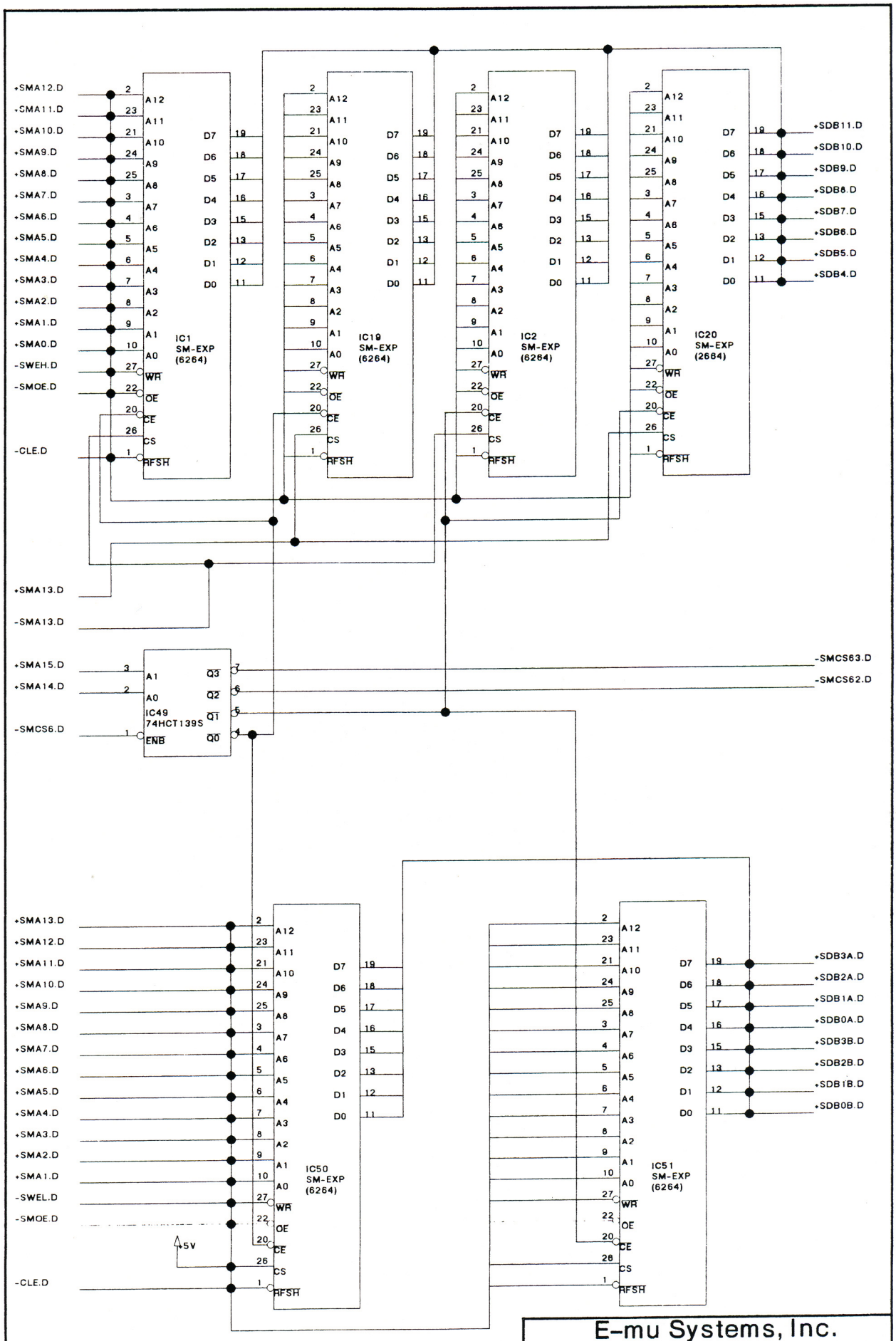
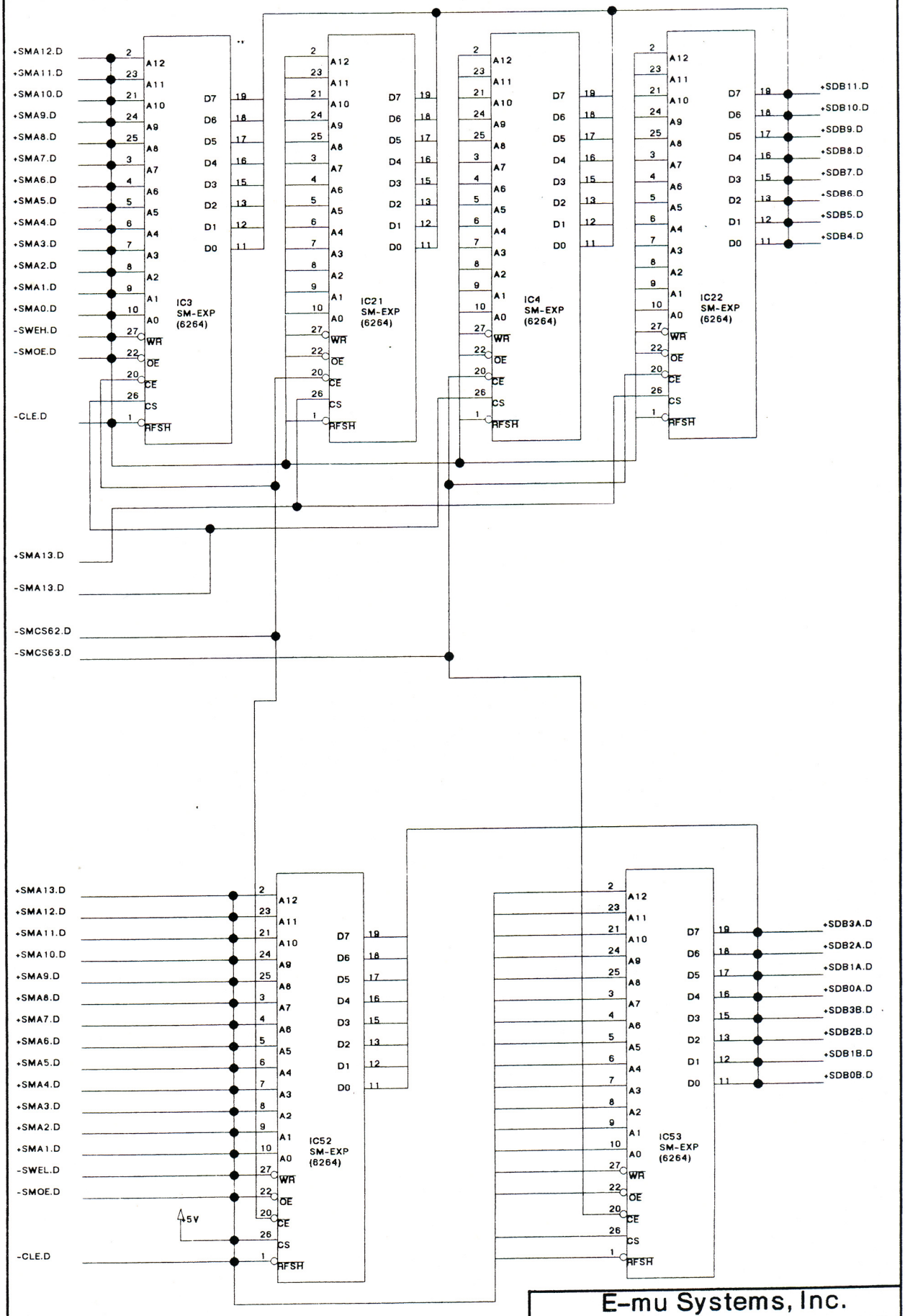


E-mu Systems, Inc.	
SP-12 Main - RAM Sound Memory	
DOC. NO. S-7600-001 PAGE 13 OF 21	7-27



E-mu Systems, Inc.

SP-12 Main - RAM Sound Memory

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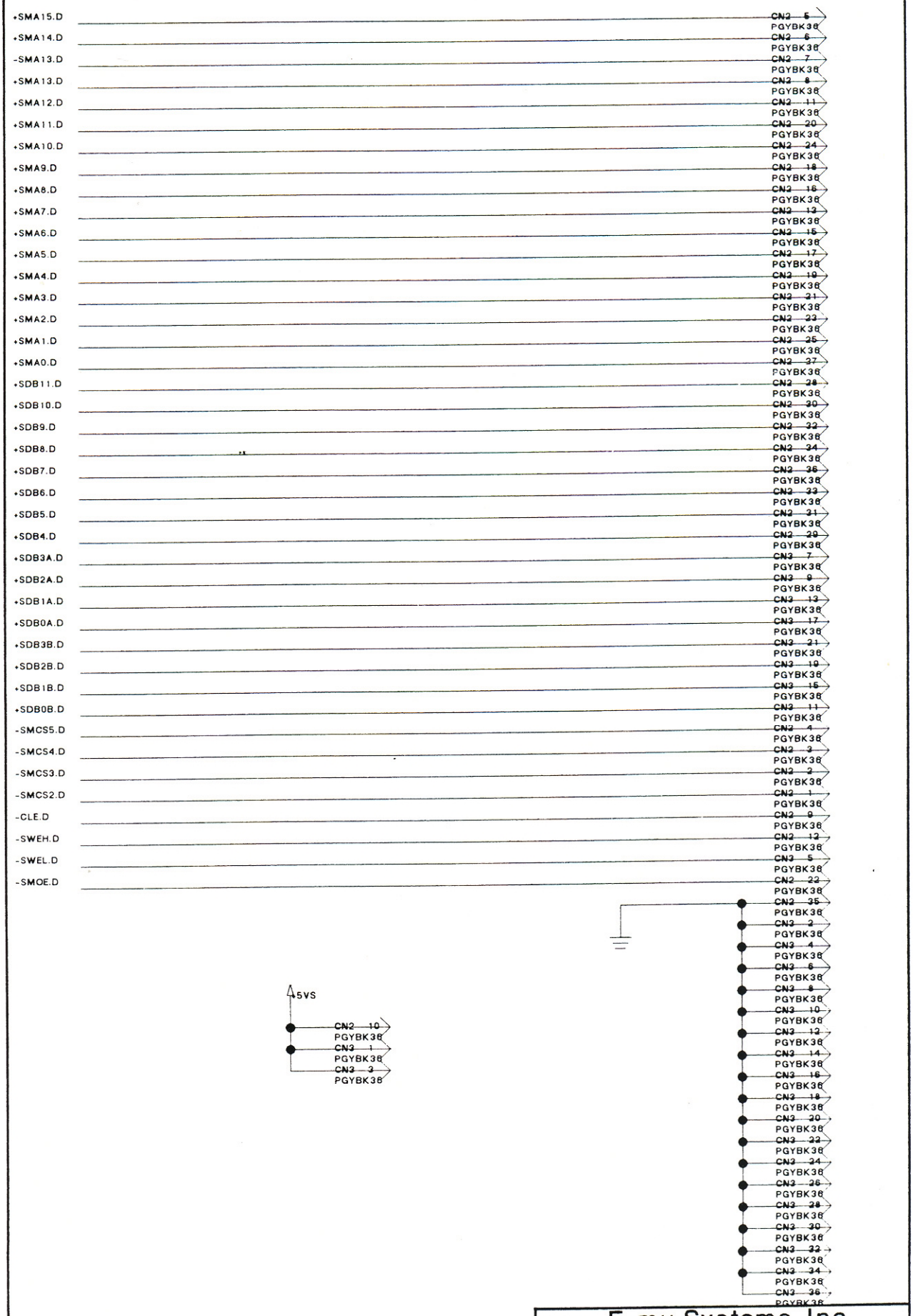
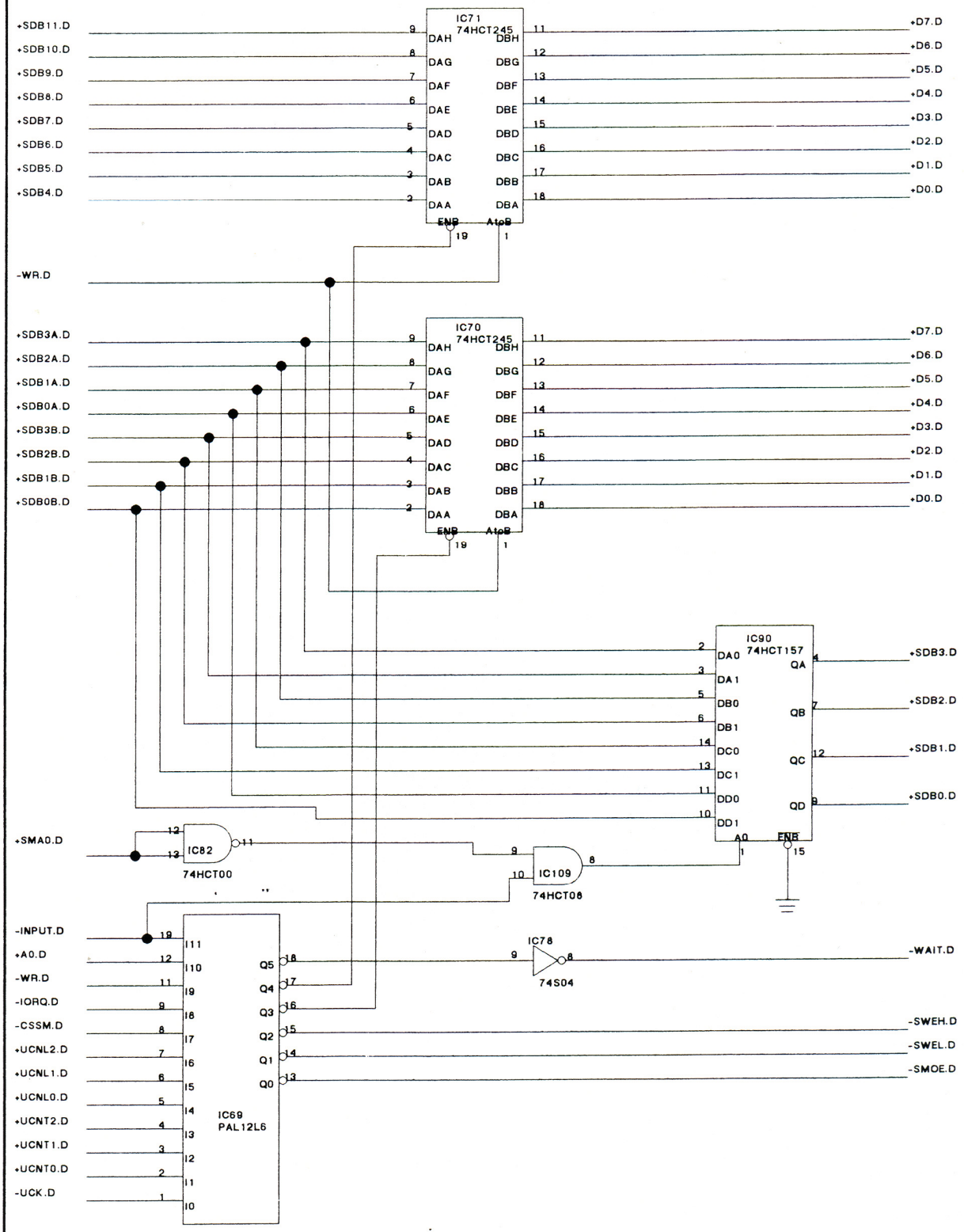
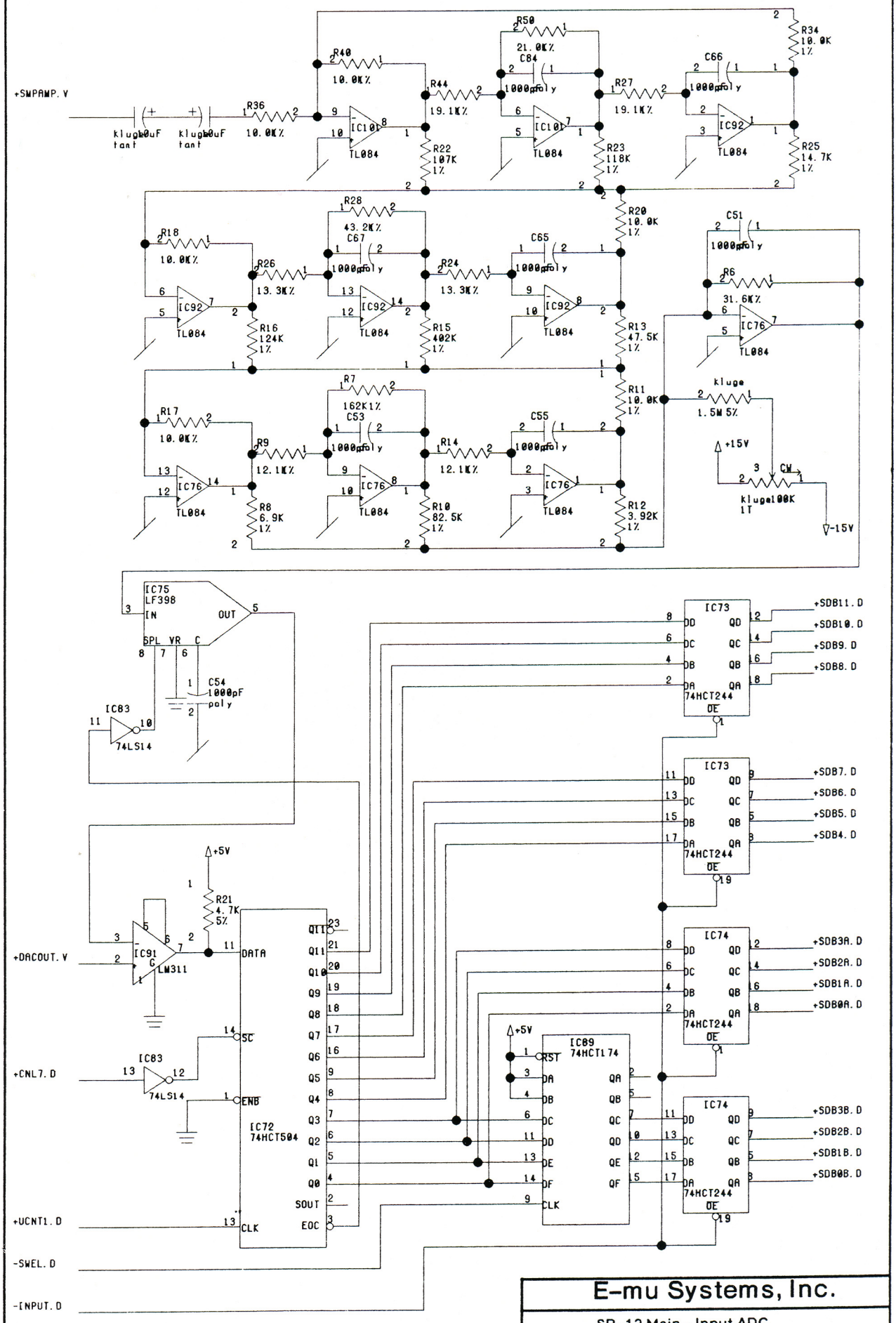


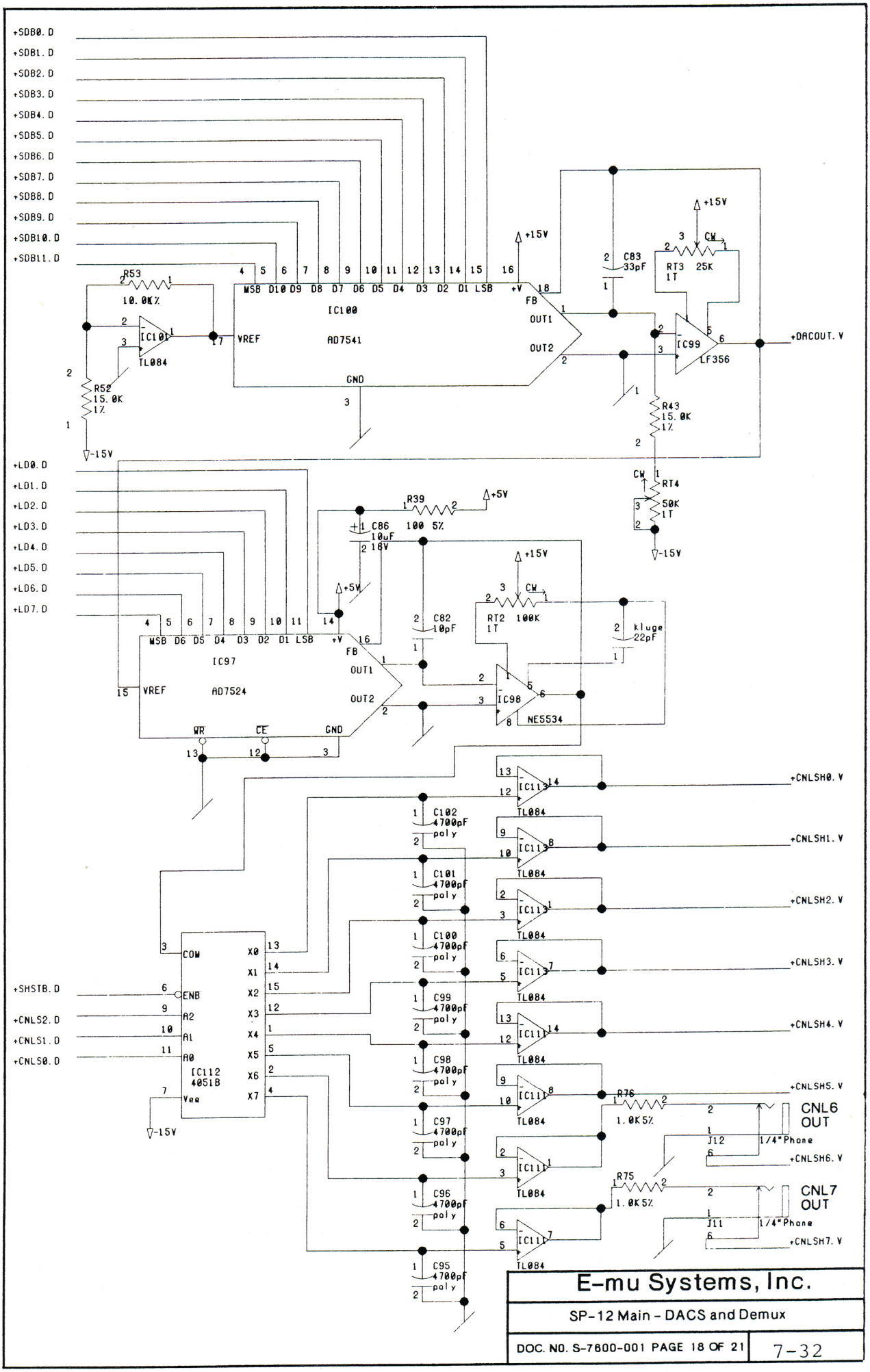
E-mu Systems, Inc.	
SP-12 - Sound RAM Expansion	
DOC. NO. S-7600-001 PAGE 15 OF 21	7-29



E-mu Systems, Inc.	
SP-12 Main - Sound Memory Intfc	
DOC. NO. S-7600-001 PAGE 18 OF 21	7-30



E-mu Systems, Inc.	
SP-12 Main - Input ADC	
DOC. NO. S-7800-001 PAGE 17 OF 21	7-31



E-mu Systems, Inc.

SP-12 Main - DACS and Demux

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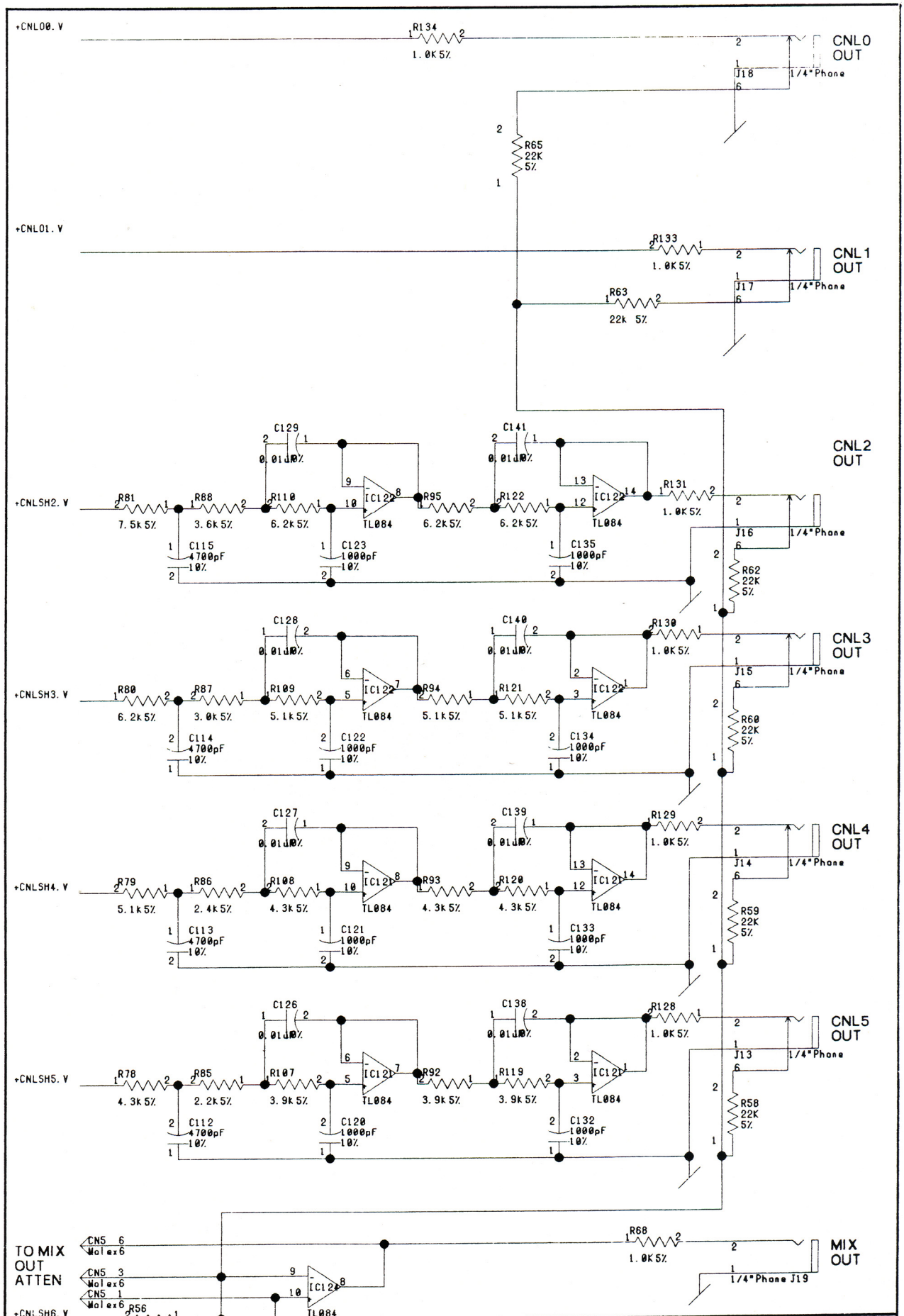
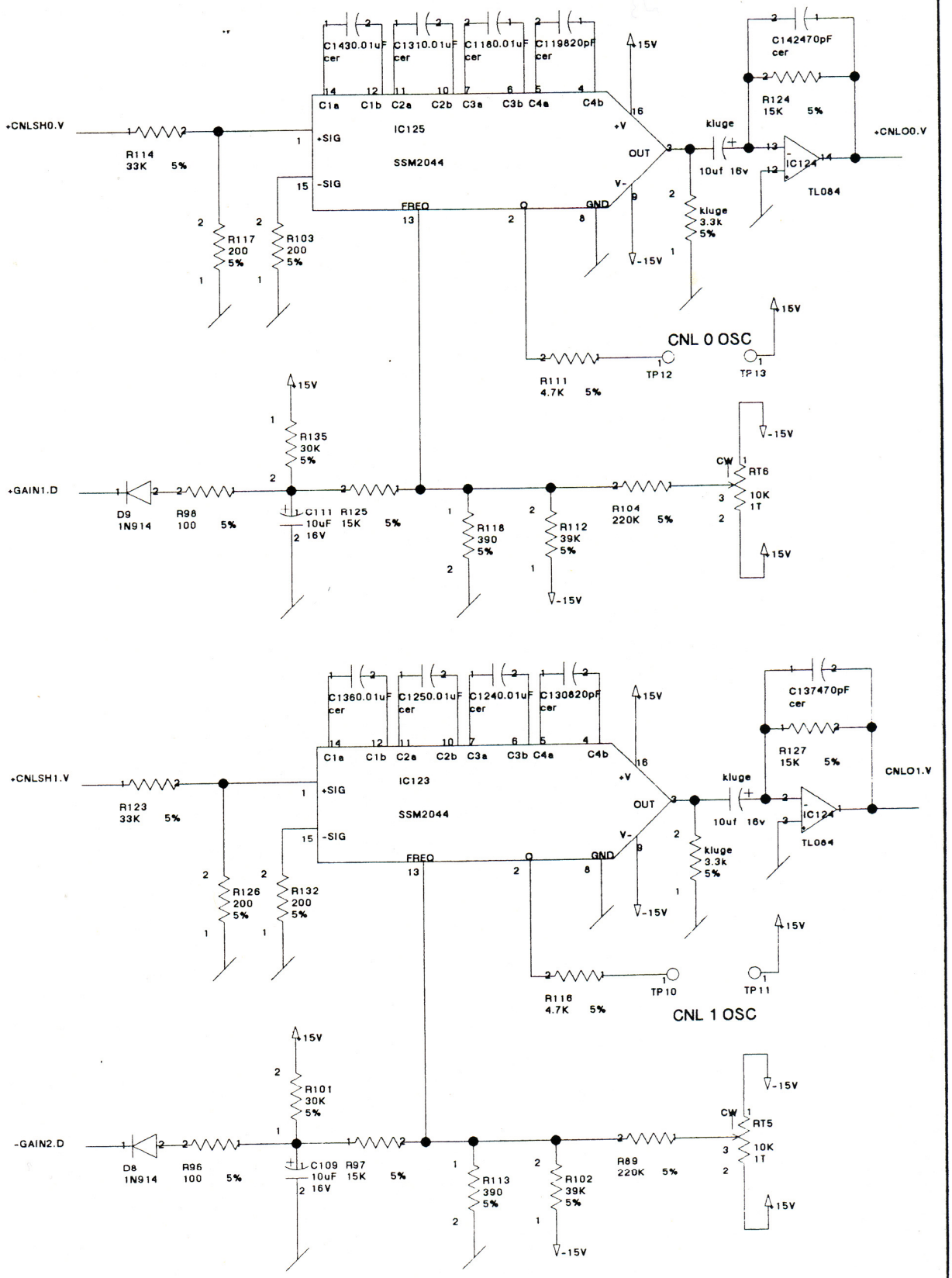
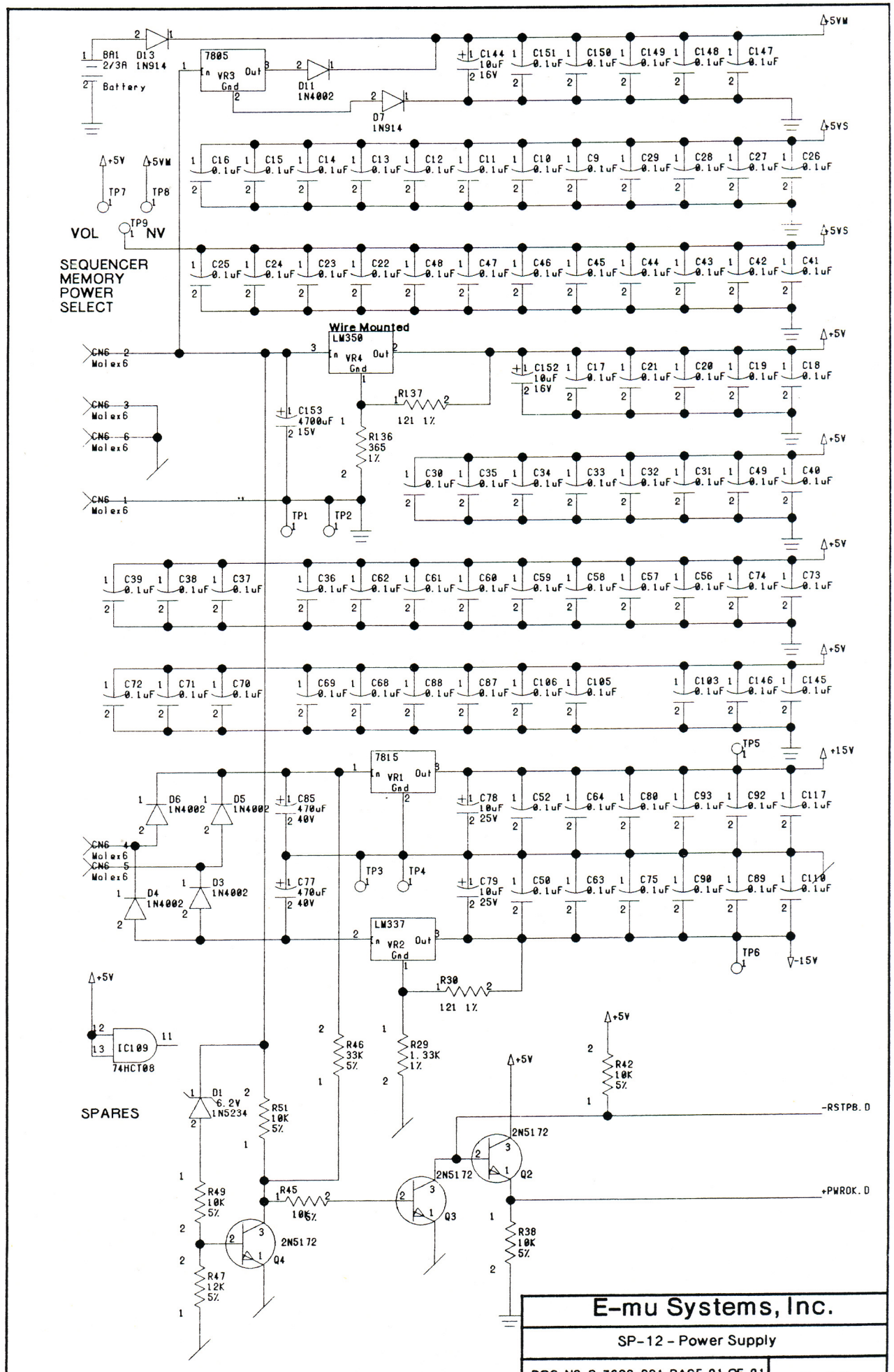


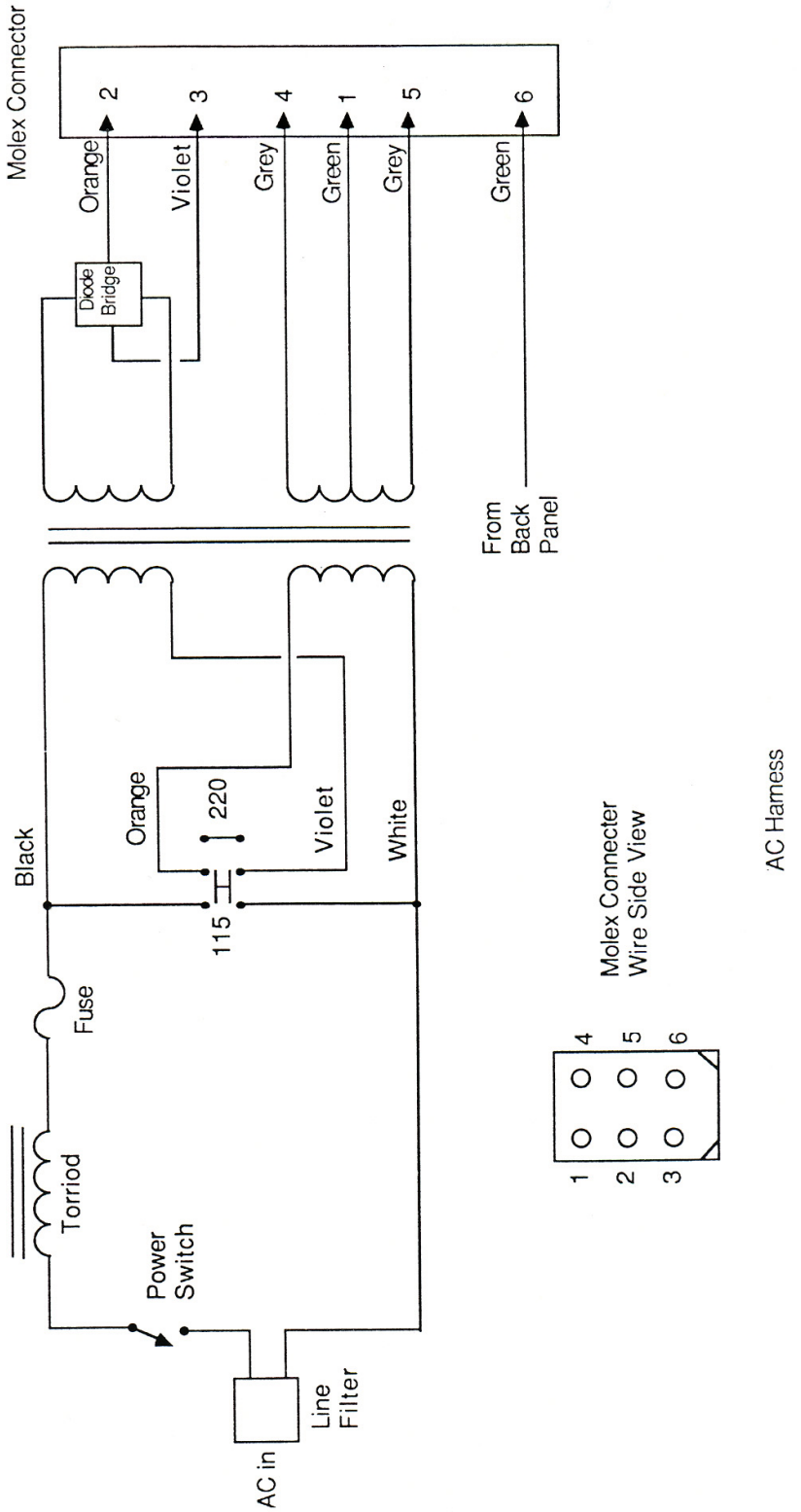
E-mu Systems, Inc.	
SP-12 Main - Output Channels	
DOC. NO. S-7600-001 PAGE 19 OF 21	7-33

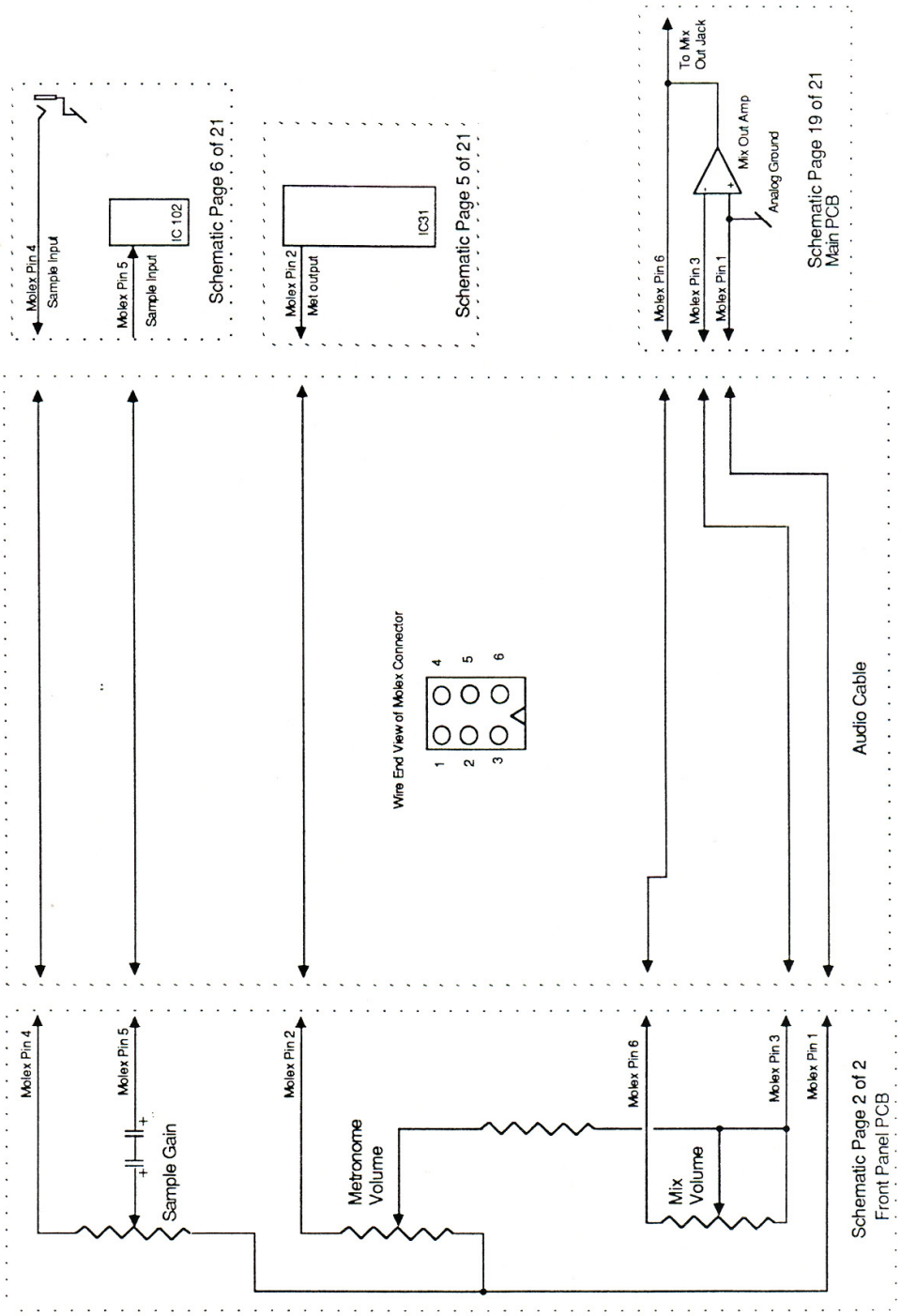


E-mu Systems, Inc.	
SP-12 Main - Dynamic filters	
DOC. NO. S-7600-001 PAGE 20 OF 21	7-34



E-mu Systems, Inc.	
SP-12 - Power Supply	
DOC. NO. S-7600-001 PAGE 21 OF 21	7-35





Value	E-mu P/N		Ref. Designator
IC Socket 18 Pin	JC105		
IC Socket 20 Pin	JC106		
IC Socket 24 Pin	JC107		
IC socket 40 Pin	JC309		
Molex PC Mnt. 6 Pin	JP111		CN5,CN6
50 Pin Ribbon Conn	JR301		CN1

INTEGRATED CIRCUITS

Analog + Hybrid ICs

6N138 Optocoupler	OE300		IC93
LM350 5 Volt Reg.	L322		VR4
4051 Multiplexer	IC208		IC112
SSM2044 4 pole filter	IL303		IC123,IC125
4053 Mux	IC345		IC102
4070	IC131		IC104
7524 MDAC	II331		IC97
ADC0809 8 input ADC	II336		IC40
7541 12 Bit MDAC	II337		IC100
TL084 Op-Amp	IL302		IC76,IC92,IC101,IC111,IC113 IC121-122,IC124
LF311 Comparator	IL102		IC91
LF356 Op-Amp	IL301		IC99
LF398 S/H	II338		IC75
NE5534	IL108		IC98

Memory ICs

2114 1Kx4 SRAM	IM357		IC13-14,IC33-34,IC43-44
2764 EPROM prog	IP338	SP12 B2	IC115
2764 EPROM blank	IM367		
27128 EPROM prog	IP337	SP12 A	IC114
27128 EPROM blank	IM367		
27256 EPROM prog	IP330	MS 1	IC9
27256 EPROM prog	IP331	MS 2	IC27
27256 EPROM prog	IP332	MS 3	IC10
27256 EPROM prog	IP333	MS 4	IC28
27256 EPROM prog	IP334	LS 1,2	IC58

Value	E-mu P/N		Ref. Designator
27256 EPROM prog	IP335	LS 3,4	IC59
27256 EPROM blank	IM358		
6264 8Kx8 SRAM	IC344		IC5-6,IC23-24,IC54-55, IC116,IC120
Digital ICs			
Z-80A CPU	IM343		IC107
Z-80A CTC	IM346		IC108
Z-80A SIO/2	IM344		IC106
74HCT00	IT369		IC82
74S04	IT375		IC78
7407	IT104		IC103
74HCT08	IT363		IC109
74HCT10	IT368		IC66
12L6 PAL	IT376		IC69
12H6 PAL	IT390		IC62
74LS14	IT307		C83
74HCT32	IT354		IC96
74HCT42	IT366		IC11
74HCT74	IT355		IC60,IC79,IC95
74HCT112	IT385		IC105
74HCT138	IT357		IC41,IC48,IC61,IC110
74HCT139	IT387		IC49
74HCT157	IT379		IC64-65,IC90
74HCT163	IT380		IC80-81
74HCT174	IT359		IC63,IC89
74LS221	IT316		IC94
74HCT244	IT360		IC73-74
74C244	IC341		IC39
74HCT245	IT383		IC70-71
74HCT273	IT361		IC29,IC30
74LS273	IT317		IC31
74LS283	IT318		IC45-46,IC15-16,IC35,36
74S288 Uc PROM	IP326		IC67
74S288 Log PROM	IP327		IC88
74LS290	IT122		IC77
74HCT373	IT362		IC12,IC17,IC32,IC37,IC47
74HCT377	IT384		IC18,IC38,IC42
74LS379	IT377		IC68
74HCT504	IT381		IC72
74HCT670	IT371		IC84-87

Value	E-mu P/N	Ref. Designator

MAIN PCB

CAPACITORS

3.3 pf	CC331	C83
5 pf	CC328	C94
10 pf	CC301	C82
22 pf	CC302	ECO 127
47 pf	CC326	C91
470 pf	CC305	C137,C142
820 pf	CC307	C119,C130
1000 pf 1KV	CC106	C107,C108
1000 pf	CC324	C120-C123,C132-C135
1000 pf Poly	CP107	C53-55,C65-67,C84,C51
4700 pf	CP108	C112-C115
4700 pf Poly	CP108	C95-102
.01 µf	CC311	C81,C126-C129,C138-C141
.01 µf 20%	CC312	C118,C124,C125,C131,C136 C143
.1 µf 20%	CC314	C1-7,C9-13,C15-50,C52,C56-64 C68-75,C80,C87-90,C92-93,C103 -106,C110,C116-117,C145-151
.1 µf 20%	CC321	C14
10 µf 16V	CT316	C86,C109,C111,C144,C152
10 µf 25V	CT317	C78-79
470 µf 40V	CA318	C77,C85
4700 µf 16V	CA319	C153

CONNECTORS

1/4" Phone Jack Mono	JA301	J5-10,J9-20
1/4" Phone Jack N/C	JA307	J11-18
IC socket 8 Pin	JC102	
IC Socket 14 Pin	JC103	
IC Socket 16 Pin	JC311	

Value	E-mu P/N		Ref. Designator
IC Socket 18 Pin	JC105		
IC Socket 20 Pin	JC106		
IC Socket 24 Pin	JC107		
IC socket 40 Pin	JC309		
Molex PC Mnt. 6 Pin	JP111		CN5,CN6
50 Pin Ribbon Conn	JR301		CN1

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4070	IC131		IC104
7524 MDAC	II331		IC97
ADC0809 8 input ADC	II336		IC40
7541 12 Bit MDAC	II337		IC100
TL084 Op-Amp	IL302		IC76,IC92,IC101,IC111,IC113 IC121-122,IC124
LF311 Comparator	IL102		IC91
LF356 Op-Amp	IL301		IC99
LF398 S/H	II338		IC75
NE5534	IL108		IC98

Memory ICs

2114 1Kx4 SRAM	IM357		IC13-14,IC33-34,IC43-44
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27128 EPROM prog	IP337	SP12 A	IC114
27128 EPROM blank	IM367		
27256 EPROM prog	IP330	MS 1	IC9
27256 EPROM prog	IP331	MS 2	IC27
27256 EPROM prog	IP332	MS 3	IC10
27256 EPROM prog	IP333	MS 4	IC28
27256 EPROM prog	IP334	LS 1,2	IC58

Value	E-mu P/N		Ref. Designator
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27256 EPROM blank	IM358		
6264 8Kx8 SRAM	IC344		IC5-6,IC23-24,IC54-55, IC116,IC120
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Z-80A CTC	IM346		IC108
Z-80A SIO/2	IM344		IC106
74HCT00	IT369		IC82
74S04	IT375		IC78
7407	IT104		IC103
74HCT08	IT363		IC109
74HCT10	IT368		IC66
12L6 PAL	IT376		IC69
12H6 PAL	IT390		IC62
74LS14	IT307		C83
74HCT32	IT354		IC96
74HCT42	IT366		IC11
74HCT74	IT355		IC60,IC79,IC95
74HCT112	IT385		IC105
74HCT138	IT357		IC41,IC48,IC61,IC110
74HCT139	IT387		IC49
74HCT157	IT379		IC64-65,IC90
74HCT163	IT380		IC80-81
74HCT174	IT359		IC63,IC89
74LS221	IT316		IC94
74HCT244	IT360		IC73-74
74C244	IC341		IC39
74HCT245	IT383		IC70-71
74HCT273	IT361		IC29,IC30
74LS273	IT317		IC31
74LS283	IT318		IC45-46,IC15-16,IC35,36
74S288 Uc PROM	IP326		IC67
74S288 Log PROM	IP327		IC88
74LS290	IT122		IC77
74HCT373	IT362		IC12,IC17,IC32,IC37,IC47
74HCT377	IT384		IC18,IC38,IC42
74LS379	IT377		IC68
74HCT504	IT381		IC72
74HCT670	IT371		IC84-87

Value	E-mu P/N	Ref. Designator
Resistors		
5% 1/4 watt unless otherwise noted		
47 ohm	RR133	R1-2
100 ohm	RR301	R39,R96,R98
121 ohm 1%	RP315	R30,R137
150 ohm	RR102	R55,R77,R82,R84,R90
200 ohm	RR302	R103,R117,R126,R132
270 ohm	RR347	R57
330 ohm DIP pack	RN320	RN1-2
330 ohm	RR303	R32
365 ohm 1%	RP313	R136
390 ohm	RR304	R113,R118
680 ohm	RR343	R19
1 kohm	RR305	R68-71,R73,R75-76,R99-100 R128-R131,R133-R134,R106
1.5 kohm SIP Pack	RN321	RN4
1.5 kohm	RR348	R38
2.2 kohm	RR337	R85
2.4 kohm	RR357	R86
3 kohm	RR327	R87
3.6 kohm	RR356	R88
3.9 kohm	RR355	R92,R107,R119
3.92 kohm 1%	RP346	R12
4.3 kohm	RR354	R78,R93,R108,R120
4.7 kohm SIP Pack	RN319	RN1
4.7 kohm	RR307	R21,R33,R48,R111,R116
5.1 kohm	RR353	R79,R94,R109,R121
6.19 kohm 1%	RP344	R8
6.2 kohm	RR352	R80,R110,R95,R122
7.5 kohm	RR351	R81
10 kohm 1%	RP106	R11,R17-18,R20,R34,R36,R40,R53
10 kohm	RR309	R3-5,R31,R35,R42,R45,R49,R51 R83,R91
10 kohm trimmer	RT301	RT5-6
11 kohm	RR310	R67
12 kohm	RR326	R47

Value	E-mu P/N	Ref. Designator
12.1 kohm 1%	RP312	R9,R14
13.3 kohm 1%	RP318	R24,R26
14.7 kohm 1%	RP349	R25
15 kohm 1%	RP107	R43,R52
15 kohm	RP311	R97,R124-125,R127
19.1 Kohm 1%	RP320	R27,R44
21 kohm 1%	RP317	R50
22 kohm	RR313	R54,R56,R58-60,R62-63,R65
25 kohm trimmer	RT307	RT3
30 kohm	RR315	R101,R135
31.6 kohm 1%	RP337	R6
33 kohm	RR316	R114,R123
39 kohm	RR317	R46,R102,R112
43.2 kohm 1%	RP323	R28
47 kohm	RR122	R72
47.5 kohm 1%	RP335	R13
48.7 kohm 1%	RP310	R41
50 kohm trimmer	RT308	RT4
82.5 kohm 1%	RP345	R10
100 kohm	RR318	R66,R115
100 kohm trimmer	RT309	RT2
107 kohm 1%	RP347	R22
110 kohm	RR342	R61
118 kohm	RR348	R23
124 kohm 1%	RP304	R16
162 kohm 1%	RP324	R7
220 kohm	RR335	R89,R104
226 kohm 1%	RP309	R37
402 kohm 1%	RP342	R15
1 mohm	RR325	R64,R74
1.5 mohm	RR332	
100 kohm trimmer	RT309	

MISCELLANEOUS

1N914 Diode	DD301	D13
1N34A germanium diode	DD304	see ECO 127
2N4121 Transistor	QQ101	Q1
2N5172	QQ302	Q2-4

Value	E-mu P/N	Ref. Designator

FRONT PANEL PCB

CAPACITORS

100 pf	CC103	C3
.02 µf	CC313	C4
1 µF	CC314	C2
1 µF 25V	CT315	C5
10 µF	CT316	C1,C6,C7

CONNECTORS

6 pin molex	JP111	CN3
50 pin ribbon conn.	JR301	CN1

Value	E-mu P/N	Ref. Designator
ICs		
4053 Mux.	IC345	IC2
TLC27M4CN Op-Amp	IL324	IC1
RESISTORS		
523 ohm	RP308	R6
4.7 kohm	RP307	R1
10 kohm Slider Pot	RC311	RT1-RT8
10 kohm LOG Pot	RC302	RT9,RT10,RT12
10.0 kohm	RP106	R7
10 kohm	RR309	R2,RT10,RT12
15 kohm	RR311	R8,R10
100 kohm	RR318	R4
100 kohm trimmer	RT309	R9
390 kohm	RR328	R11
2.2 mohm	RR338	R9
SWITCHES		
Play pushbutton	SW301	SW3-SW12
Pushbutton Red	SW306	SW1,SW37
Pushbutton Blue	SW302	SW2,SW13-36,SW38-40

Value	E-mu P/N	Ref. Designator
MISC.		
1N914 Diode	DD301	D1-41
LED Red	LP302	LP1-15
LCD Display	LP304	
4-40 3/8 Screw	HS302	
3mm x 10 mm Phlps scrw	HS325	
4-40 Nut	HN304	
3/8 32 Nut for Pot	HN311	
Nylon Spacer for Slider	HS305	
Nylon Spacer on Display	HW210	
14 Wire Flexstrip	WW313	CN2
Power Supply for LCD	ZV300	ZV300
Piezo Crystal	ZX303	
BOTTOM PANEL		
AC Receptacle	JP129	
AC Power Cable	AD334	
Transformer	ZT307	
115/220 switch	SW107	
Diode Bridge 50V 5 Amp	DB300	
Line filter		
Female Molex		
AC Power Switch		
Fuseholder		
Rubber feet		
Screw		
Nut		