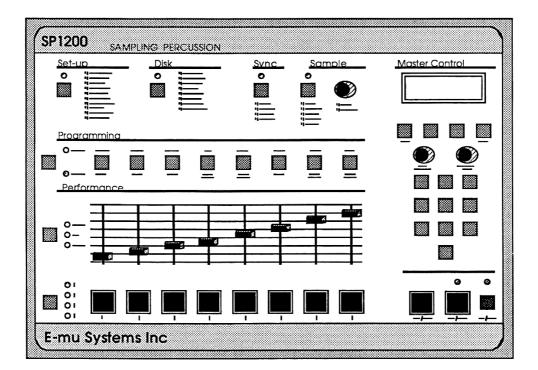
# SP1200 SAMPLING PERCUSSION SYSTEM



# SERVICE MANUAL

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### **INTRODUCTION** 1

### INTRODUCTION

The SP1200 Digital Sampler is a powerful and complex instrument. E-mu Systems Inc. intends this manual to be an aid to the experienced service technician only.

To service the SP1200 you should be familiar with the 7400 series of digital logic, floppy disk drives, ADC's and DAC's, op-amps as well as microprocessor troubleshooting techniques, and current music synthesizer technology. The minimum equipment required to service and repair the SP1200 are: a digital multimeter, a 100MHz dual trace oscilloscope and basic technician hand tools.

Because the SP1200 has so many complex functions, we highly recommend having a complete <u>SP1200 Operation Manual</u> on hand to help you understand all the functions.

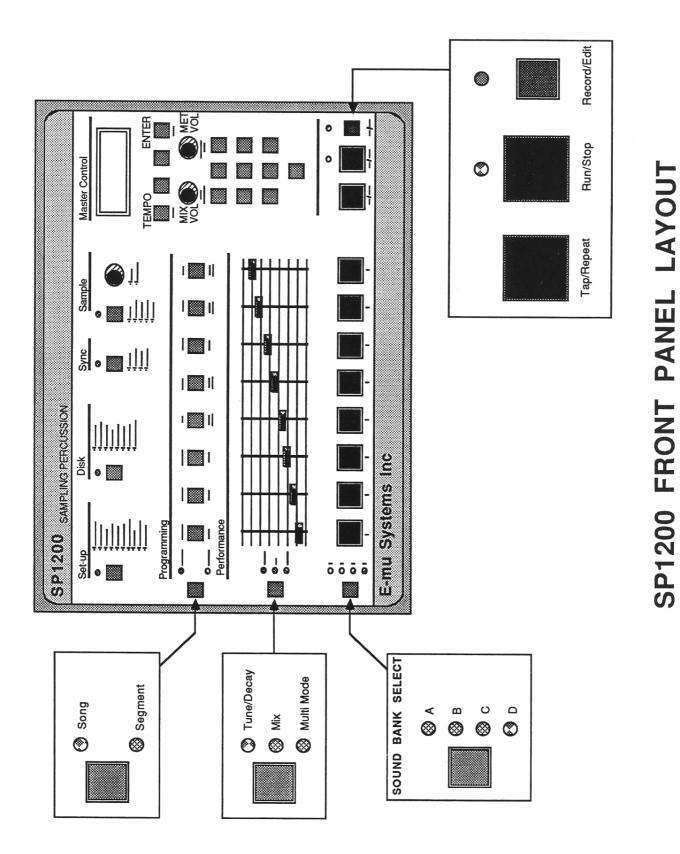
The information contained in this manual is proprietary to E-mu Systems Inc. The entire manual is protected under copyright and none of it may be reproduced by any means without written permission from E-mu. This manual is available only to approved service people and is property of E-mu Systems. Please consider all of the data secret and use it only to service the SP1200.

We feel obliged to remind you that any modification of an SP1200 other than as specified by a factory authorized E-mu Change Order (ECO) will void the warranty of the instrument.

Please read this manual thoroughly before attempting to service the SP1200. If you feel unsure about working on the instrument, contact our service department.

# **BASIC OPERATION**







## <sup>4</sup> BASIC OPERATION

### **BASIC OPERATION**

These brief instructions are not meant as a substitute for the <u>SP1200</u> <u>Operation Manual</u>. To completely understand the operation of the SP1200 we strongly recommend that you have a complete manual on hand. The <u>SP1200 Operation Manual</u> can be ordered through our Customer Service department.

The panel is divided up into 7 modules. Each module has a specific group of functions. The Performance Module has all the real time controls, such as the Play Buttons, sequencer Run/Stop and Record. The sliders have multiple functions as selected by the TUNE/DECAY, MIX, MULTI MODE button. The play buttons are assignable by pressing SELECT. TAP/REPEAT is used to enter a desired tempo by tapping the button (in tempo mode) or repeat a sound being played automatically.

**MASTER** The Master Control Module has a backlit LCD display as well as a numeric keypad and ENTER button. The TEMPO button is used to change the current tempo value. Right and left arrow buttons increment or decrement the value above the flashing cursor. YES and NO buttons let you make decisions and the Mix and Metronome output levels are set here.

**PROGRAMMING** To the left of the master control is the Programming Module. The creation of songs and segments is the function of this module. In Segment mode the selection of auto correct, time signature, segment length and metronome rate are controlled here. Step programming and segment copy as well as swing functions are controlled by Segment Mode. Song Mode is used for creating songs by linking segments together. Mix and tempo changes are controlled here.

**SET-UP** Above and to the left is the Set-Up Module. It has the controls for all of the multi-modes such as Multi-pitch and Multi-level. It also has channel assignments for routing sounds to different output channels and Loop/Truncate for modifying sounds that have been sampled. Deleting sampled sounds as well as changing their decay are initiated using this module. MIDI parameters are selected and the Special Function section contains all the functions not on the front panel and any that have been added as software updates.

**DISK** To the right of Set-Up is the Disk Module. All Disk operations such as loading, saving and formatting disks are initiated through this module.

### BASIC OPERATION 5

**SYNC** Next is the Sync Module. This is used for selecting the method of clocking the sequencer. The options are: Internal Sync, where the internal sequencer clock is the master. MIDI, where the MIDI clock triggers the sequence. SMPTE, which uses an audio SMPTE track and Click, which uses a square wave type sync track on tape, another drum machine or a sync box.

**SAMPLE** Last we have the Sample Module. This allows the user to sample up to 32 of their own sounds. The SP1200 has 10 seconds of sampling time which is divided up into (4) 2.5 second banks. That is, no one sound can be longer than 2.5 seconds. After being sampled the sound can be truncated, looped, decayed or pitch shifted and assigned to any output channel.

#### PROGRAMMING OVERVIEW.

The SP1200 has two main programming modes, **Segment** and **Song**. Segments are drum patterns that can vary in length from 1 to 99 measures. The user creates Segments that contain the songs introduction, main groove, fills and the ending. The Segments are then linked together in Song Mode to create the song. Song and Segment modes are selected by pressing the Song/Segment mode select button. When Song mode is selected, the horizontal row of programming buttons assume the functions along the top Song row. When Segment mode is selected, the buttons assume the lower Segment related functions.

### PERFORMANCE OVERVIEW

All the sounds are accessed through this module. Only eight sounds at a time can be played. Which eight are played can be accessed by using the **Select Button**. It is possible to "rip off" a sound by playing two sounds at the same time when they are assigned to the same output channel. The software assigns the last sound played as the priority. This can be used to a good effect on the Hi-Hat to simulate the foot opening and closing it. It can also cause problems if you try to play two sounds at the same time on the same channel.

The TAP/REPEAT button is used for entering a tempo or repeating a sound. In Tempo mode the button is tapped several times to enter the desired tempo. Repeat is used for automatically repeating a sound at the Auto Correct rate. This is done by holding the repeat button down and pressing the desired sound.

### INTERFACE SPECIFICATION

### THE MIDI INTERFACE

**Hardware:** MIDI is a serial, 5 milliamp current loop interface between two or more computer controlled musical instruments. It uses optoisolators and non-grounded inputs to prevent ground loops. MIDI operates at a 31.25K Baud rate and does not use any handshaking. Each MIDI connection requires two wires to complete the loop. The hardware used is very simple. The output is an open collector driver, consisting of a 7407 and a series resistor. The return line is a series resistor connected to 5 volts. The MIDI input current runs through a 150  $\Omega$  resistor and then directly into a 6N138 optoisolator. The SP1200 uses the standard 5 pin DIN connectors for MIDI IN, MIDI OUT and MIDI THRU.

**MIDI Thru:** MIDI Thru on the SP1200 is an open collector driver, consisting of a 7407 and a series resistor.

**System Exclusives:** SP1200 contains MIDI system exclusive commands in the form of MIDI Sample Dump commands. For more information on the system exclusive specifications, refer to the MIDI specification at the end of this section.

### SMPTE INTERFACE (Society of Motion Picture and Television Engineers)

To understand SMPTE a very basic knowledge of video is extremely helpful. If you do not understand video, we suggest finding a book or two on the subject of SMPTE and Video. SMPTE time code is used primarily for editing video tape. It is recorded on a spare audio track and has a 80 bit code that uniquely identifies each frame. The format looks like this:

|Hours|Minutes|Seconds|Frames|

SMPTE has other uses such as syncing two 24 track tape machines together or film to sound syncing. It is also used in studios as the master sync track and for autolocators on multitrack tape machines. Since SMPTE records the absolute value, it is superior to click tracks and regular sync tones. The SP1200 sequencer can be programmed to start at 1 hour, 20 minutes, 30 seconds, 21st frame and it will start precisely at that moment. If the master tape is fast forwarded, the SP1200's sequencer will fast forward until sync is achieved then begin

## <sup>8</sup> INTERFACE SPECIFICATION

playing. It will also send a MIDI Song Pointer command from it's MIDI out so that other MIDI devices can lock to SMPTE. There are two SMPTE transmission rates we use. For video in the USA, 2400 baud is used. This number is derived from 30 frames per second times 80 bits per frame. For most of the rest of the world 2000 baud is used. This corresponds to 25 frames per second times 80 bits. Film uses 24 frames per second and gets by using 2000 baud. The SMPTE input needs to see at least 250 millivolts to read the time code reliably. For more information on how we generate and receive SMPTE, see the Theory of Operation.

### **CLOCK IN and CLOCK OUT**

**Clock In:** The SMPTE/Clock in jack allows an external device such as another drum machine or sequencer to control the tempo of the SP1200. The SP1200 can receive almost any input clock rate by the use of its software clock divider (in the Sync module). The SP1200 is based on 24 ppn. The input circuit reads changes of state, therefore to read a 24 ppn clock, the divisor should be set to divide by 2. The divisor can divide from 1 to 99 and thus can read clock rates from 12 to 1188 pulses-per-quarter note. The pulses should be **at least 1 millisecond wide and have a level of 1 to 5 volts.** 

**Clock Out (Met):** The metronome out jack allows SP1200 to be the master clock and drive sequencers and drum machines at a rate of 24 pulses per quarter note. The SP1200's metronome can be programmed to output 24 ppn in either song or segment mode. This is a **5 volt pulse which is about 6 milliseconds wide.** 

### CASSETTE IN

The SP1200 will read SP-12 cassette data files. Both sequence and sound data can be transferred. See Appendix I in the <u>SP1200</u> <u>Operation Manual</u> for detailed instructions on transferring data.

### FOOTSWITCH AND PEDAL CONNECTION

**Footswitch:** Three control footswitch jacks are provided for performance control of Run/Stop, Single Step, or Tap Tempo. The footswitches should be of the **momentary contact type** and should be **normally-open**.

### AUDIO CONNECTIONS

**1. Mono:** The SP1200 has provisions for a variety of output connection schemes. The most common hookup will be simply to use the Mix out jack. If a monophonic amplifier is used, simply connect the Mix output to the input of the amplifier. Guitar amps are not recommended because they are generally noisy and low fidelity. The output level of SP1200 is somewhere in between instrument and line level. Care should be taken when connecting to an instrument amplifier so that the delicate nerve cells in your ears are not destroyed.

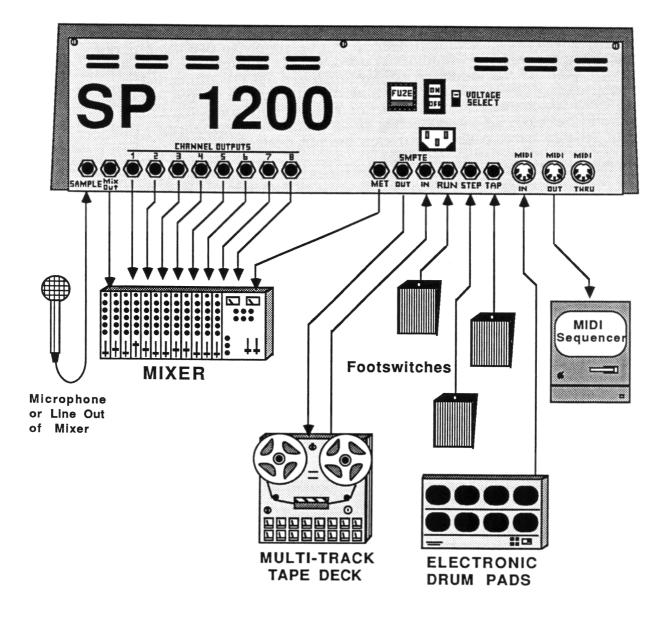
**2. Individual Outputs:** There may be times when different equalization or reverb settings are desired on the various instruments that have been sampled. SP1200 has eight monophonic channel outputs that can be used when individual processing on specific instruments is desired. Voices are assigned to output channels using the channel assignment function in the Setup module. Dynamic Allocation defeats the channel assignments. Note that the Mix Output is summed from the individual outputs. Output impedance is  $1 \text{ K} \Omega$ .

**3. Sample Input:** The sample in jack can accept any signal level from microphone level to line level. The gain is adjusted with the sample input pot and the cursor keys while in VU/gain mode in the sample module. The level can be read in the liquid crystal display while in this mode. Input impedance is  $10K \Omega$ .

### AC POWER CONNECTION and FUSE

The AC power connector is how SP1200 gets power (obviously). The fuse receptacle is just as obvious. It is located directly next to the power receptacle. Before changing or checking a fuse, UNPLUG the power cord. To remove the fuse holder, simply press in the red fuse cap. The fuse holder will now pop out with it's fuse in the fuse socket. **SP1200 uses a 1 amp, 250 volt fast-blo mini-fuse.** SP1200 should not normally blow fuses. If a fuse that has been replaced blows again, suspect the transformer or diode bridge.

## <sup>10</sup> INTERFACE SPECIFICATION



## SP-1200 Rear Panel Connection Diagram

### SP1200 MIDI Implementation Copyright E-mu Systems inc. 1987 5/21/87

X = item implemented

- = item not implemented

MIDI command	Transmitted?	Received?
Note off	х	Х
Note on	Х	Х
Poly key pressure	-	-
Control change	-	-
Program change	-	-
Channel pressure	-	-
Pitch wheel	-	-
Sustain footswitch	-	<u>-</u>
Local control on/off	-	-
All notes off	-	Х
Omni mode	-	Х
Mono mode	-	
Poly mode	-	Х
Song position pointer	Х	X
Song select	Х	Х
Tune request	-	-
Timing clock	Х	Х
Start sequence	Х	Х
Continue sequence	Х	Х
Stop sequence	Х	Х
Active sensing	-	-
System reset	-	-
System exclusives	Х	Х

Note: All numbers in HEX, except numbers in parenthesis, which are DECIMAL.

### **TRANSMITTED MESSAGES: Basic MIDI Commands**

Note On/Off ("Pitch Keys" off)	9n kk vv kk 00	n = MIDI channel no. (0 to 15) kk = key# (36 to 67) velocity (loudness) kk = key# (36 to 67) zero velocity for note off
Note On/Off ("Pitch Keys" on)	9n 40 kk VV kk 00 pp 00	n = MIDI channel no. (0 to 15) pp = pitch key# (69 to 83) nominal velocity (64) kk = key# (36 to 67) velocity (loudness) kk = key# (36 to 67) zero velocity (key's note off) pp = pitch key# (69 to 83) zero velocity (pitch key's note off)

Note Ons are followed immediately by note off, running status, zero velocity.
 Velocity is fixed at 7c unless "dynamic buttons" is on, in which case the velocity value will vary from 0c to 7c.

<ul> <li>Song Position Pointer</li> <li>LL and mm make up a 14 bit num MIDI beats (1 beat = 6 MIDI clock the song.</li> <li>Sent by SP1200 when Sync is se is received. Will fast-forward to th segment and output the appropria</li> <li>After sending a Song Position Po command.</li> </ul>	s = one s t to SMF e approp ate song	sixteenth note) since the start of PTE, and a new SMPTE time code priate place in the song or position value over MIDI.
Song Select	f3 ss	ss = song # (0 to 99)
Sent by SP1200 when a new sor		0

### **Timing Clock**

f8

 $\Box$  Sent by the SP1200 when sequence is running, unless Sync is set to MIDI, in which case Timing clocks are not sent by the SP1200.

Start

fa

 $\Box$  Sent by the SP1200 when a song is started from the front panel.

### Continue

fb

 $\Box$  Sent by the SP1200 only after a Song Position Pointer is sent.

Stop

fc

 $\Box$  Sent by the SP1200 when a song is stopped from the front panel.

### TRANSMITTED MESSAGES: MMA Sample Dump Commands

MMA stands for MIDI Manufacturer's Association, the organization that invented the "Sample Dump Standard".

Dump	Request	f0 7e	system exclusive
		ch	MIDI base channel (0 to 15)
		03	MMA exclusive number
		SS	sound number lsb (0 to 31)
		00	sound number msb (always 0)
		f7	EOX
⊑> s	P1200 will only send this if it	is request	ted to do so from the front panel

Special function (24). (See "Receiving a sound dump".)

# Transmitting a sound dump from the SP1200 to an external device with the MMA Sample Dump Standard.

- There are two ways an SP1200 can be made to transmit a sound dump over MIDI:

- SP1200 can receive a "Dump Request" exclusive from an external device, (hereafter called the "Requestor", specifying a sound number (0 to 31). - Manually, from the front panel "Special" function (23).

- SP1200 first checks if the requested sound exists (size not = 0):

- doesn't exist: request is ignored, nothing happens.

- does exist: continue.
- SP1200 responds by displaying "Sending Sound Data over MIDI" on it's LCD.
- SP1200 then sends the "MMA sample dump header", telling requestor among

other things, how big of a sample to expect.

- SP1200 then polls it's MIDI input line, waiting for a response from requestor within SP1200's timeout period of 5 seconds.

- If response is an ACK, (packet # ignored) SP1200 will continue dump.

- If response is a WAIT, SP1200 will reset it's timeout counter (5 seconds), and go back to waiting for a response again. If requestor needs more time to make up it's mind, it should send more Wait commands.

- If no response at all, SP1200 will assume an "open loop" system and continue the dump.

- If response is anything else, it is bad, and SP1200 will display "Sound Dump Bad, Press Enter", then send a CANCEL command, and abort back to normal SP1200 operation.

- SP1200 now switches it's timeout from 5 seconds to about 20 mS.

- SP1200 will then send the sound dump in a series of "MMA Data Packets", starting with packet # 00. After Requestor receives packet, it responds:

- If response is an ACK, SP1200 will continue dump with next packet. An ACK response must have the correct packet # . Packet numbers continue up thru 7f, then wrap around back to 00.

- If response is a WAIT, SP1200 will reset it's timeout counter (20 mS), and go back to waiting for a response again.

- If response is a NAK, SP1200 will try sending the same packet again. - If no response at all, SP1200 will assume an "open loop" system and continue the dump.

- If response is anything else, it is bad, and SP1200 will display "Sound Dump Bad, Press Enter", then send a CANCEL command, and abort back to normal SP1200 operation.

- SP1200 will continue sending packets, getting an ACK for each one, until it has sent the entire dump, as specified by the "sound length" in the Sample Dump Header.

- The last packet will always contain 120 data bytes, even if there may be fewer than that remaining in the sound. The remaining bytes will be filled in with garbage data and should be ignored.

- After sending the last packet, SP1200 displays "Sound Dump Good Press Enter", and returns to normal operation.

- Every 8 packets sent, SP1200 will toggle an asterisk on the LCD.

MMA Sample Dump Head	7e Oc 01 ss 00 Oc	system exclusive MIDI base channel (0 to 15) MMA exclusive number sample number lsb (0 to 31) sample number msb (always 0) significant bits (12)
	02	sample period (Isb) in nsec

S
)
j)
)
)
`

Sample period is fixed at (1/26.04)kHz = 9602 HEX in nanoseconds.

**MMA Data Packet** fO system exclusive 7e 0c MIDI base channel (0 to 15) 02 MMA exclusive number CC packet count (0 to 127) 120 data bytes ---------XX checksum (exclusive OR of above 124 bytes) f7 EOX The (120) data bytes represent (60) 12-bit linear SP1200 data words: byte 0: Obbbbbbb bbbbbbb = 7 ms bits of data word 0byte 1: 0aaaaa00 aaaaa = 5 Is bits of data word 0 0ddddddd byte 2: dddddd = 7 ms bits of data word 1byte 3: 0000000 ccccc = 5 is bits of data word 1 -----etc----yyyyyy = 5 ls bits of data word 59 byte 119: 0yyyyy00 The 12-bit data is in "complement offset binary" format: most negative value = 000 hex, "zero" = 800 hex, most positive = fff hex Acknowledge (ACK) fO system exclusive 7e 0c MIDI base channel (0 to 15) 7f packet number pp f7 EOX

 $\Box$  See "Receiving a sound dump" description.

Not Acknowledge (NAK)	f0 7e 0c 7e pp f7	system exclusive MIDI base channel (0 to 15) packet number EOX
See "Receiving a sound dum	p" descript	ion.
Cancel Dump (CANCEL)	f0 7e	system exclusive
	0c 7d	MIDI base channel (0 to 15)
	pp f7	packet number EOX

 $\Box$  See "Receiving a sound dump" description.

Note Off	8n kk vv	n = MIDI channel # (0 to 15) kk = key # (36 to 67) vv = velocity (1 to 127) ignored
Note Off	9n kk 00	n = MIDI channel # (0 to 15) kk = key # (36 to 67) zero velocity
Note On If SP1200 receives a Note Of "pp" before it gets a Note Off for "		
All Notes Off and Mode Messages	bn mm 00	n = MIDI channel # (0 to 15) mode command (123 thru 127)
<ul> <li>All mode messages (123 thru 127) turn off notes whose source was MIDI.</li> <li>□&gt; If mode number was 123, 126, or 127, SP1200 will only do the all notes off.</li> <li>□&gt; If mode number was 124, SP1200 will also set POLY mode.</li> </ul>		

### **RECEIVED MESSAGES: Basic MIDI Commands**

## INTERFACE SPECIFICATION 17

□ If mode number was 125, SP1200 will also set OMNI mode.

Song Select       f3         SS       SS = sequence # (0 to 99)         Image: Receiving this selects a new sequence on the SP1200.         Timing Clock       f8         Ignored unless Sync is sent to MIDI.         Advances SP1200's sequencer by 1/96th note.         Ignored if SP1200 is waiting for a Continue after receiving a Song P Pointer.         If received while SP1200 is fast forwarding after receiving a Song P Pointer and a Continue, the Song Position cue point will just be incremented by one.	ent song or segment. It will then ing Clocks before starting to play
<ul> <li>Ignored unless Sync is sent to MIDI.</li> <li>Advances SP1200's sequencer by 1/96th note.</li> <li>Ignored if SP1200 is waiting for a Continue after receiving a Song P Pointer.</li> <li>If received while SP1200 is fast forwarding after receiving a Song Pointer and a Continue, the Song Position cue point will just be</li> </ul>	
	Ignored unless Sync is sent to M Advances SP1200's sequencer Ignored if SP1200 is waiting for Pointer. If received while SP1200 is fast Pointer and a Continue, the Son
Sequencer Start fa	incremented by one.
Sequencer Stop fc	

### **RECEIVED MESSAGES: MMA Sample Dump Commands**

Dump Request	f0 7e	system exclusive
	0c 03	MIDI base channel ( 0 to 15) MMA exclusive number
	SS	sample number lsb (0 to 31)

00 sample number msb (always 0) EOX

 $\Box$  Upon receiving this, SP1200 will stop whatever it is doing and attempt to transmit an MMA sound dump of the specified sample. (See "Transmitting a sound dump" description.)

f7

 $\Box$  The sound number must be between (0 and 31), or else it is ignored. The "sound number msb" must always be 0. Sound 0 will replace the sound at A1 on the SP1200, and sound (31) will replace sound D8.

➡> MIDI base channel is ignored.

### Receiving a sound dump from an external device to the SP1200 with the MMA sample dump.

There are two ways an SP1200 can be made to receive a sound dump over MIDI:

- SP1200 can receive a "Sound Dump Header" exclusive from an external device, (hereafter called the "Sender"), specifying a sound number (0 to 31). - Manually, from the front panel "Special" function (24), which sends a

"Dump Request" out MIDI for the specified sound. This may or may not cause a sound dump, depending on what the SP1200 is connected to.

- The sound being received will replace the existing sound in the SP1200, so the first thing the SP1200 does is check if the specified sound exists:

- If sound doesn't exist, (size = 0), SP1200 aborts, nothing happens.
- If sound length is non-zero, dump continues.

SP1200 then displays "Receiving Sound Data over MIDI" on it's LCD.

 $\Box$  SP1200 then sends an "ACK" (with packet# = 00, although Sender should ignore), to let Sender know that header was received OK.

⇒ SP1200 will now poll it's MIDI input line, waiting for data packet #00.

 $\Box$  Sender should then send the sound dump in a series of "MMA Data"

Packets", starting with packet # 00. After SP1200 receives packet, it responds: ACK, if packet was not garbled and packet # and checksum were correct.

SP1200 will then wait for the next packet.

CANCEL, if anything but an ACK is seen, or nothing at all is seen within the timeout period of 5 seconds. SP1200 then displays "Sound Dump Bad, Press Enter", and returns to normal operation.

□ If Sender sends a WAIT instead of a data packet. SP1200 will reset it's timeout counter (5 seconds) and look for the same packet again.

Note that SP1200 will accept only as many bytes as are currently allocated for that sound in the SP1200. If fewer than that many are sent, SP1200 will fill the remainder with silence. If more than that are sent, SP1200 will send CANCEL on the last packet it cares about, and ignore any subsequent packets.

☐ If all packets received OK, SP1200 will display "Sample Dump Good Press Enter" and return to normal operation. If something was bad, SP1200 will display "Sample Dump Bad Press Enter", and return to normal operation. - Every 8 packets sent, SP1200 will toggle an asterisk on the LCD.

fO

Sample	Dump	Header
--------	------	--------

system exclusive

7e	
0c	MIDI base channel (0 to 15)
01	MMA exclusive number
SS	sample number lsb (0 to 31)
00	sample number msb (always 0)
0c	significant bits
рр	sample period (Isb) in nsec
рр	sample period (nsb)
рр	sample period (msb)
LL	sample length (Isb) in words
LL	sample length (nsb)
LL	sample length (msb)
SS	sustain loop start word (Isb)
SS	sustain loop start word (nsb)
SS	sustain loop start word (msb)
ee	sustain loop end word (Isb)
ee	sustain loop end word (nsb)
ee	sustain loop end word (msb)
Lt	loop type
f7	EOX

 $\Box$  "MIDI base channel" is ignored.

 $\Box$  The sound number must be between (0 and 31), or else it is ignored. The "sound number msb" must always be 0. Sound 0 will replace the sound at A1 on the SP1200, and sound (31) will replace sound D8.

SP1200 uses the "significant bits" to determine how to decode the Data Packets (see "MMA Data Packet" description below).

SP1200 ignores the "sample length". Instead it will accept only as many bytes as are currently allocated for that sound in the SP1200. If fewer than that many are sent, SP1200 will fill the remainder with silence.

Sample period is ignored, since SP1200 has only one playback rate, 26.04 kHz.

 $\Box$  Sustain "loop start" and "loop end " are ignored. The original sound's loop points are used instead.

"Loop type" is ignored, since SP1200 only has one loop type, forwards.

ММА	Data	Packet	f0 7e	system exclusive
			7 e	

#### 20 INTERFACE SPECIFICATION 0c MIDI base channel (0 to 15) 02 MMA exclusive number CC packet count (0 to 127) 120 data bytes ... •• checksum of above 124 bytes XX f7 EOX $\Box$ The MIDI base channel is ignored. rightarrow The 120 data bytes are packed according to the "significant bits" in the sample dump header. There are 3 possible data packet configurations: - for # significant bits = (8 thru 14): The (120) data bytes represent (60) 14-bit linear data words: byte 0: 0bbbbbbb bbbbbbb = bits (7 thru 14) of data word 0 byte 1: 0aaaaaaa aaaaaaa = bits (0 thru 6) of data word 0Oddddddddddddd = bits (7 thru 14) of data wordOcccccccccccccc = bits (0 thru 6) of data word 1 byte 2: ddddddd = bits (7 thru 14) of data word 1 byte 3: -----etc----byte 119 Oyyyyyyy yyyyyy = bits (0 thru 6) of data word 59 - for # significant bits = (15 thru 21): The (120) data bytes represent (40) 21-bit linear data words: bvte 0: 0000000 ccccccc = bits (15 thru 21) of data word 0 byte 1: bbbbbbb = bits (7 thru 14) of data word 0 Obbbbbbb 0aaaaaaa byte 2: aaaaaaa = bits (0 thru 6) of data word 0 byte 3: 0 fffffff fffffff = bits (15 thru 21) of data word 1 Oeeeeee byte 4: eeeeeee = bits (0 thru 6) of data word 1 -----etc----byte 119 Oyyyyyyy yyyyyy = bits (0 thru 6) of data word 39 - for # significant bits = (22 thru 28): The (120) data bytes represent (30) 28-bit linear data words: byte 0: Odddddd ddddddd = bits (22 thru 28) of data word 0 byte 1: 00000000 ccccccc = bits (15 thru 21) of data word 0 byte 2: bbbbbbb = bits (7 thru 14) of data word 0 Obbbbbbb 0aaaaaaa byte 3: aaaaaaa = bits (0 thru 6) of data word 0 byte 4: Ohhhhhhh hhhhhhh = bits (22 thru 28) of data word 1 byte 5: ggggggg = bits (15 thru 21) of data word 1 Oggggggg -----etc----byte 119 Owwwwww wwwwww = bits (0 thru 6) of data word 29

While the SP1200 will accept any of these formats, in all cases it will only use the (12) most significant bits of each data word and ignore all the rest.

Acknowledge (ACK)	f0 7e 0c 7f pp f7	system exclusive MIDI base channel (0 to 15) packet number			
f7 EOX ➡ MIDI base channel is ignored. ➡ See "Transmitting a sound dump"					
Not Acknowledged (NAK)	f0	system exclusive			
	7e 0c	MIDI base channel (0 to 15)			
	7e pp f7	packet number EOX			
➡ MIDI base channel is ignored. ➡ See "Transmitting a sound due	.,	LOX			
Wait (WAIT)	f0	system exclusive			
	7e 0c	MIDI base channel (0 to 15)			
	7c pp f7	packet number EOX			
$ \stackrel{\square}{\Longrightarrow} MIDI \text{ base channel is ignored.} $ $ \stackrel{\square}{\Longrightarrow} \text{ See "Transmitting a sound due} $					

# **MECHANICAL PROCEDURES**

### MECHANICAL PROCEDURES 23

### MECHANICAL PROCEDURES

### PRECAUTIONS

Observe the following precautions when working on the SP1200:

Switch power off and check 110/220 switch before connecting SP1200 to power outlet or amplifier.

NEVER toggle the 110/220 switch with power on.

Troubleshooting must be done with power on.

Do not bend or strain the PCBs or you may cause tiny breaks in the printed circuit traces which will be very difficult to find.

Switch power off before disconnecting or connecting any circuitry, or removing or installing PCBs.

To replace soldered components, switch power off, remove the PCB completely from the instrument, and desolder from both sides. Use a vacuum desoldering tool. The traces on the SP1200 circuit boards are very thin. Use extreme care and work carefully. Remember: Heat the pin, <u>not</u> the pad.

### Opening the SP1200

### THE SERVICE POSITION

Before taking the SP1200 apart we recommend providing a soft work surface. A carpeted or rubber covered workbench is ideal. When the machine is in the service position the front panel will be face down on the work surface which might damage it. We also recommend the use of an extra long interpanel cable (50 pin ribbon) which will allow you to place the top panel face up next to the bottom panel. This will prevent top panel scratches while allowing access to the front panel and the main PCB inside the unit.

To open the unit place the SP1200 upside-down on the padded workbench and remove the (5) screws (E-mu P/N HS364) from the perimeter of the bottom panel. Flip the machine right side up and

## 24 MECHANICAL PROCEDURES

remove (3) screws (E-mu P/N HS364) from the top edge of the back panel. Grasp the top panel at it's thickest portion and lift it as if there were a hinge at the front. This is analogous to opening the cover of a large book. The top cover will pivot about 180 degrees and lay face down on the padded work surface. The front panel PCB is connected to the main PCB via a short 50 pin ribbon cable. This cable can be removed from either or both ends. As previously mentioned, replacing this cable with one that is about 2 feet long will make working on the machine much easier. These cables can be found at electronics and computer stores or through mail order.

### **REMOVING THE FRONT PANEL PCB**

First remove the 50 pin ribbon cable and audio cables, Next remove the knobs from the front panel by pulling on them. Lay the top cover face down on a soft work surface and remove the 12 screws E-mu P/N HS 353) and lift out the PCB. If any parts need replacement the fisch paper will have to be removed. Note that the inside cover is coated with a conductive material. The fisch paper keeps the circuitry from shorting to this coating. To install the PCB, reverse the above procedure.

### **REMOVING THE MAIN PCB**

Unplug the 50 pin ribbon and audio cables. Remove the nuts and washers on the back panel jacks and put them in a safe place. Unplug the AC harness from the PCB. Remove the hex nut and washer that attaches the 5 Volt regulator to the back panel. Remove the 8 screws holding the PCB in place and carefully remove the PCB. To install, reverse the procedure. It's OK for the regulator to be shorted to the back panel, but make sure that it's tightened down securely and has heat sink compound applied.

### **REMOVING THE FLOPPY DISK DRIVE**

To remove the floppy disk drive, first remove the power and data cables from the floppy drive. The drive is mounted to the bottom panel housing by (4) 4-40 x 1/4" machine screws (E-mu P/N HS 352).

### FUNCTIONAL TEST

This Functional test is designed to test all of the functions without taking the machine apart. Everything can be tested using this procedure but it is not as quick in some cases as using the built-in ROM diagnostics. These tests can be used in addition to the ROM diagnostics when the results of a test are questionable.

You will need a pre/power amp or receiver with a speaker or headphones to accomplish the functional test.

If the sound tests give questionable results the DAC trims (see diagnostics) could be the culprit.

**1. LED Test**. All the LEDs are turned on for a second when power is first applied. Check to see that all of them are lit.

**2. Display.** The display has 2 lines of 16 characters. If you can read both lines of the sign on message then the display is probably OK. We haven't seen many display failures, and don't expect you will see problems very often. If one fails, replace the whole assembly.

3. Button Test. Test the sound buttons by pressing each one and listening for a sound. Make sure dynamic buttons are on, then hit the play buttons hard and the sound will get louder. If it does not, the dynamic button circuit could be at fault. Test the SELECT button by pressing it and looking to see if the LED that is lit is advanced by one. The TUNE/DECAY and SONG/SELECT buttons are tested similarly. Press the SET-UP button and check that it's LED comes on. The DISK. SYNC and SAMPLE buttons are tested in the same way. To test the TEMPO button press SONG/SEGMENT button to get into either one of those modes. Press TEMPO and check that the blinking cursor on the display is now under the tempo value. Now press the left arrow button and check that the tempo value decreases. Press the right arrow button and the tempo value should increase. Press the ENTER button and the blinking cursor on the display will move to a position under the song/segment number. Pressing any keypad number twice will change the song/segment number to a two digit value corresponding to the button pressed. To test the TAP/REPEAT button press and hold it while pressing any sound play button and listen for the sound repeating continuously. The rate of repeat will be determined by the auto-correct setting. Test the RUN/STOP button by pressing it while in segment mode. One of two things should happen. If the segment

selected has a sequence in it, the SP1200 will begin playing. If the segment was empty the metronome will beep. To test RECORD get into song mode by pressing the SONG/SEGMENT button. Now press RECORD and the LED should light.

**4. Sound Test.** You should listen to all the sounds critically at the mix out jack and at their separate output jacks. Plugging into the separate outputs will remove that sound from the mix output. Listen for excessive noise or distortion, clicks or pops and any other abnormalities. If any one or two sounds are bad, check to see if they share an output channel (Channel Assign). If they do then that channel's output filter or sample/hold is suspect. If all sounds are bad check the separate channel out. If they sound good here then the mix out amp is suspect. If they are still bad check the Main DAC, the Level DAC and their buffers. If nothing looks bad use the ROM diagnostics and check the Sound RAM. Also listen to the metronome output by plugging into the met out jack and running a sequence. This is a full level output so be careful.

**5.** Slider Test. Press the TUNE/DECAY button twice to call up MIX mode. The display will show a bar graph for each slider corresponding to the sound level during playback. Before testing the sliders note the position of the bar graph so it can be restored to it's original position. Test each slider by moving it to the maximum and minimum position while watching the display. At minimum only one segment will be seen. At maximum all the segments will be seen. Adjust the slider until the bar graph is returned to the original position. Test the remaining sliders in the same way.

**6. Potentiometer Test.** To test the mix out pot start a sequence by pressing RUN/STOP. Turn the pot through it's full range listening for noise or dropout. Test the metronome pot by creating a segment with no sounds playing. To do this, find a blank segment or erase one. Press RECORD and hold it, then press RUN/STOP. You will now hear the metronome clicking at quarter note intervals. Turn the metronome pot through it's entire range listening for noise or sound dropout. When the pot is set to minimum, no sound should be heard. Noise on these pots can indicate either a dirty pot or DC offset on the line.

To test the sample pot it will be necessary to erase some of the sample memory. To erase sound memory press SET-UP, 23, 15 and YES. this will erase all of the sound memory. Now press SAMPLE. You will need a signal source to sample. The radio, a synthesizer or a signal generator will work. Connect the audio source to the sample input. Press sample and adjust the input level by pressing 3 and then using the right and left arrow select 0, 20 or 40 dB. Set the input level so

that the gain pot can be set near maximum and the VU meter does not go off scale. Press 9 to start sampling and turn the sample pot from it's maximum to minimum position during the sampling period. Press sample to exit the module. Press SELECT next to the play buttons until LED A is lit. Play the A1 button and listen to the sample. Listen for a steadily decreasing level with no pops, clicks or sound dropout.

**7. Disk Test.** You will need a blank  $3.5" \mu$ floppy diskette for this test. Insert the blank disk in the drive and select the DISK module. Press 9 for Format/Copy Software. The display will say Format Disk: Are You Sure? Say YES and the display will say: Formatting... After the disk has been formatted you can save the contents of the machine to disk and then load them back in which will verify the disk functions. If the disk fails any of these tests invoke the ROM diagnostic routines.

**8. MIDI Test.** To test MIDI a keyboard or drum machine that is MIDI equipped will be needed. Connect the SP1200's MIDI OUT to the other unit's MIDI IN. If using a keyboard, select a patch that has a fast attack on the envelope. Hit a few play buttons on the SP1200 while listening to the other machine. Does it play? If it does then the SP1200's MIDI transmit is OK. Now connect the SP1200's MIDI IN to the other unit's MIDI OUT. Play a few keys (at the lower end of the keyboard) while listening to the SP1200. If it plays the MIDI receive circuits are functioning properly. If this test fails try running the ROM diagnostics.

**9. SMPTE Test.** You will need a tape deck to perform these tests. A multitrack deck is ideal because it allows you to simulate an actual studio situation, however a stereo deck will suffice for the basic test.

#### **Basic Test**

We will write a SMPTE track on tape, rewind the tape and trigger the sequencer with the SMPTE track we just made. Plug the SP1200's SMPTE OUT jack into your tape deck input. Start the tape recording. Press SET-UP, 23, and 14. Adjust the record level to -3 VU. Let it run for about a minute. Press ENTER to stop the SP1200 and rewind the tape to the beginning. On the SP1200 press SYNC 3, then press ENTER 3 times. Get into segment mode and press RUN/STOP to play a segment. The display should tell you that it is "Awaiting SMPTE". Plug the tape deck output into the SMPTE IN. Start the tape and watch the display. When SMPTE is received and decoded the display will change and replace the "Awaiting SMPTE" message with the SMPTE time display which shows (numerically):

#### HH:MM:SS:FF

Where HH = hours, MM= minutes, SS = seconds, FF= frames

The frames display will be changing fast enough to be difficult to read. The sequence should be playing as well.

#### **Advanced Test**

For this test you need a multitrack recorder.

- 1. Record a simple segment 2 bars long into the SP1200.
- 2. Stripe the tape with a few minutes of SMPTE code.
- 3. Set the SMPTE start point to about 00:00:15:00
- 4. Setup the SP1200 for SMPTE as explained above.
- 5. While syncing to SMPTE, record the sequence on another track.
- 6. Rewind and listen to the live SP1200 track vs the recorded track. They should stay in perfect sync. Let it run for awhile.
- 7. Pull out the SMPTE cord and plug it back in. The SP1200 should catch up and lock on perfectly.

Problems? Try adjusting the signal level entering the SP1200. If there are still problems call Emu Customer Service. They might be able to help.

**10. External Footswitches.** You will need a momentary normally-open footswitch that terminates with a 1/4" plug. Alternately any 1/4" cord can be used and one end can be shorted using a suitable conductor. Plug the switch into the RUN/STOP jack. This should start and stop the sequencer when the footswitch is pressed. Plug the footswitch into the STEP/END REPEAT jack. Press the SONG/SEGMENT button to get into song mode. Watch the display while you press the switch and you should see the song number advance. Plug the footswitch into the TAP/AUTO REPEAT jack. Press and hold the footswitch while holding a play button. The sound should retrigger continuously as long as the switch is held down.

# **DIAGNOSTICS AND TRIMS**

### **DIAGNOSTICS** 29

### **DIAGNOSTICS and TRIMS**

The SP1200 contains a number of on-board diagnostic tests and trim procedures. These can be accessed or read from the front panel without even opening the unit!

### SP 1200 DIAGNOSTICS

To activate the diagnostic software, power the instrument up while holding SETUP depressed, or press SETUP before a disk has been inserted.

The instrument will perform a series of tests as outlined below. To step from test to test, press ENTER. This will be prompted when screen size allows. It is safe to turn the instrument off during any test.

The tests are:

- 1. CPU RAM Test
- 2. ROM Test
- 3. Sound RAM Test
- 4. Button/Footswitch Test
- 5. LCD Test
- 6. LED Test
- 7. Slider Test
- 8. Sample Trim Test
- 9. MIDÍ Test
- 10. SMPTE Test
- 11. Dynamic Button Test
- 12. Disk Test

Exiting the disk test cycles the unit back to the Button/Footswitch test; the user must reboot to repeat the RAM and ROM tests.

The details of each test are as follows:

#### 1. CPU RAM TEST

Tests the CPU dynamic RAM with a fairly uncomprehensive test from location 2000H to FFFFH. Will catch all gross failures. Reports error address and IC # of failure. Press ENTER to step to next test.

## 30 DIAGNOSTICS

### 2. ROM TESTS

Calculates and displays the ROM checksum which should be identical to that displayed by PROM programmers. Prompts you to press ENTER to step to the next test.

### 3. SOUND RAM TEST

Uses a fairly comprehensive double pass pattern to test the CPU access of the sound RAM. Reports error address and IC #. Press ENTER to step to the next test. This test takes a couple of minutes.

### 4. BUTTON/FOOTSWITCH TEST

Displays the name of the button or footswitch on the display when pressed. Pressing ENTER displays "enter" and steps to the next test on the release of ENTER.

### 5. LCD TEST

Displays "boxes" on the display to verify that all dots work. Press ENTER (you guessed it) to step to the next test.

### 6. LED TEST

Gives LED chase pattern. Provides hours of entertainment. Prompts you to press ENTER to step to the next test.

### 7. SLIDER TEST

Displays De-jittered value (0-127) on 8 sliders. Press ENTER to step to the next test.

### 8. SAMPLE TRIM TEST

Prompts for adjustment of RT1 (sample offset) to a value of 800. The actual value is displayed. Should be adjusted near to, but not exactly 800 (797-->803). Press ENTER to step to the next test.

### 9. MIDI TEST

Prompts for a loopback connection from MIDI IN to MIDI OUT, and to press ENTER when connected. MIDI is tested for all possible bytes, and the results reported. Press ENTER to step to the next test. Pressing <-- repeats the MIDI test.

#### **10. SMPTE TEST**

Prompts for a loopback connection from SMPTE IN to SMPTE OUT, and to press ENTER when connected. SMPTE is tested for all possible bytes at rates of 30 and 24 FPS (this takes about 5 sec), and the results reported. Press ENTER to step to the next test. Pressing <-- repeats the SMPTE test.

## **DIAGNOSTICS** 31

### **11. DYNAMIC BUTTON TEST**

Reports dynamic button sensor result (0-200) for all play buttons. Adjust the trimmer on the back of the front panel board for maximum dynamic range. This adjustment is non-critical. Adjust to customer's preference. Press ENTER to step to the next test.

### **12. FLOPPY DISK TEST**

Prompts to press 1 for verify only test, 2 for write/verify test (WARNING: DESTROYS ALL DATA ON THE DISK), 3 to skip back to CPU RAM test.

A verify test reads all tracks on a previously written disk and reports errors for each full pass. A write/verify test writes a pseudo-random pattern onto all tracks of the disk, verifying after each write, then reads the disk in its entirety and reports errors from both passes. Holding "3" down at the end of a pass exits the test.

Errors are reported as follows:

PASS	HE	DE	SE	<b>P1</b>
NNNN	NN	NN	NN	NN

Pass is the pass number; a write/ verify pass is counted as a single pass. Up to 9999 passes (about 70 hours) will be logged before weirdness occurs.

**HE** is the number of hard (uncorrectable after 10 retries) errors that occurred during the test. Note that DISK NOT READY from an uninserted disk is considered a hard error, as is WRITE PROTECT if write/verify is chosen.

**DE** is the number of CRC errors that occurred. It takes 10 in a row to generate a hard error.

**SE** is the number of seek errors that occurred. It takes 2 on a row to generate a hard error.

**P1** is the number of "phase one" errors that occur. Since the drive attempts to read the disk before the settling times have elapsed, counting on the CRC and seek error detection to find any errors, this displays any such errors that occur. Failures on this test does not indicate a "bad" drive. They mean that the drive is not in perfect alignment and will take longer to load a disk since it has to re-read tracks.

**HE**, **DE**, **SE**, and **P1** display a maximum of 99 errors, and will continue to display 99 when more than 99 errors have occurred. It is safe to remove the disk at any time from a VERIFY test; no damage will result to the diskette. Removing the diskette during a WRITE/VERIFY test may write a bad sector on the disk (preventing it from being useful for a verify test subsequently); powering the instrument down may even de-format the diskette. We recommend you either use one diskette only for WRITE/VERIFY tests, or that you hold "3" down to exit the test before powering the instrument down.

#### POWER SUPPLY SPECIFICATIONS

The SP 1200 power supply generates 4 voltages: +5 V, +15 V, -15V, and +12 V. The specifications are:

VOLTAGE	TEST POINT	SPECIFICATION
+5V Digital	Any TTL Chip	4.75 to 5.25 Volts
+15V Analog	Pin3 VR1 or TP	14.25 to 15.75 Volts
-15V Analog	Pin3 VR2 or TP	-14.25 to -15.75 Volts
+12V Analog	12V TP near Reg.	11.25 to 12.75 Volts

#### TRIM PROCEDURE

The SP 1200 has 7 trimmers located on the main circuit board. Four of the trimmers are trimmed using a high impedance digital ohm meter. These relate to the DC offset adjustments around the sound and level DACs. The sample offset trim (RT1) is calibrated by using the diagnostic routine #8. The last two trims are the dynamic filter trims and can either be calibrated using an oscilloscope or to personal taste by using your ears.

The DAC DC offsets can and do drift over time and should be routinely checked to ensure optimum performance.

#### To Calibrate the DAC trims:

1. Turn on the SP 1200 and let it warm up for about 15 minutes.

2. Turn the unit OFF then reboot without playing any buttons.

3. Attach the GROUND lead of your ohm meter to the analog ground (TP 3 and 4) on the circuit board.

4. Adjust the trimmers using the test points given in the order listed.

#### 1st DAC OUTPUT LEVEL TRIM (Use Oscilloscope)

This adjusts the maximum gain of the DAC buffer so that the 4051 demultiplexer will not be overdriven which causes distortion and channel crosstalk. The gain trimmer is RT7.

To trim RT7: Playback various samples with dynamic buttons OFF, all mix levels FULL and with scope probe on IC98 pin 6. Trim RT7 so that the level out of IC98 does not exceed 5 Volts peak-to-peak. Listen to the audio outputs afterward with the SP 1200's mixer up full to make sure that no clipping or crosstalk is occurring.

#### OHM METER TRIMS

	TRIMMER	TEST POINT	SPECIFICATION
2nd	RT3	IC99 pin 2	Less than 1 millivolt
3rd	RT4	IC99 pin 6	Less than 1 millivolt
4th	RT2	IC98 pin 2	Less than 5 millivolts
Any Order	RT1	SP 1200 Diagnostics	Reading of ≈804 or greater in the display. (Should not be exactly 800)

Test the RT1 trim setting by entering Sample mode with no input and gain set at +40 dB. Turn up your amp gain and listen for a clicking noise at the mix out. If you hear clicking, readjust RT1.

**5th** Recheck RT7 and recalibrate if necessary.

**Dynamic Filter Trim:** 

#### Factory method

1. Short the two test points CNL0 and CNL1 which puts the filters into oscillation.

2. Tune the output frequency of each filter to 1.0 kHz. Monitor at pins 1 and 14 of the TL084 output buffer or Mix Out jack with volume full.

#### By ear method

1. Simply play tom-tom drum sounds through channels 7 and 8 and adjust the tone to taste. The customer may even want these outputs to be brighter or duller. Ask them.

In any case, the filter adjustments are non-critical.

#### SMPTE PROBLEMS

Problems related to SMPTE (or sync problems in general) seem to be a constant source of grief. Actually they are not that hard to solve if you know how to go about it. SMPTE problems seem to have 3 major causes: Ground loops, One-shot problems and of course *operator error*.

Ground Loops. Ground loops in computer audio equipment can have more symptoms than just the familiar 60 cycle hum. Digital audio ground loops can take the form of high frequency whines and tones caused by the beating of digitally generated signals. These tones can adversely affect the SMPTE track as well as adding unwanted noise to the audio chain. Ground loops are formed when interconnected pieces of equipment have more than one path to ground. They are usually caused by having the 3rd prong of each power cord plugged in to the socket. Since these are all common and the ground wire of the audio cords are common, two or more ground paths are set up. A general rule for eliminating ground loops is to 3-wire ground only one piece of equipment in the system, usually the mixer or power amp. Unfortunatly this defeats the safety feature of the 3-prong cord and voids the warranty of most equipment. It can and does solve many sync and noise problems. Use of a direct box when recording the SMPTE track can also be of help in getting a clean signal on tape.

**One-Shot Window.** One-shots always seem to cause trouble and this circuit is no exception. The componants age and change value and then the circuit doesn't work correctly. If a customer is having SMPTE sync problems, the test below is a good place to start. If the window is out of spec, the capacitor (C81) can be replaced or the resistor value (R41) adjusted as necessary. Remember to set your scope for negative slope trigger when performing the measurement.

#### SMPTE One-Shot Test

We have found that the timing Cap. on the One-Shot circuit is often not within tolerance.

To check for the proper pulse width;

1) Feed a 2.5Khz square wave of at least 250mv into the SMPTE input.

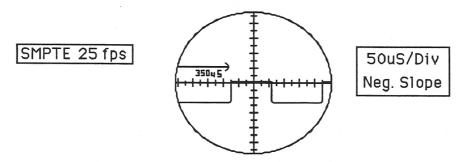
2) Set SP-1200 for SMPTE sync at 25 frames per second.

3) Set up scope for 50 us/div and a negative trigger.

4) Measure pulse width at IC 94 pin 12. It should be between 300 and 370 us.

5) Set SP-1200 for SMPTE sync at 30 frames per second

6) Measure pulse width at IC94 pin 12. It should be between 250 and 300 ys.



**SP1200 Tempo.** The tempo of the SP1200 is not *exactly* as shown in the display. It is close enough for most uses but we have had cases where it was not close enough. Case in point. SMPTE was written with another SMPTE generator and a sequencer track recorded. The SP1200 was brought in later to add the drums but the tempos didn't match. A basic drum track should have been recorded first and the sequencer synced to the SP1200. There would have been no problems.

Make sure the SMPTE start point is set later than 00:00:00:00. The SP1200 needs a few frames to lock on.

### COMMON SP 1200 PROBLEMS

When troubleshooting the SP 1200, we recommend checking the power supply first. Other common sources of problems are connectors, sockets, and broken solder joints. You should also make sure that you are using the latest version of software to avoid chasing phantoms. If you suspect a software problem and you are using the latest version, contact the factory. The most frequent problems seem to be with the disk drive which is not normally field repairable.

If you get stuck on a problem, please feel free to contact our Customer Service department at (408) 438-1921. They will be happy to assist you. Telephone support hours are between 8:30 am and 5:30 pm PST Monday through Friday.

PROBLEM	CAUSE	SOLUTION
<b>No Boot</b> No lights, no power	Power Supply problem	Check it out!
No Boot No Diagnostics	Bad RAM PAL	Replace RAM PAL
Won't boot-up disk	Check ICs 126,127 are from	same manufacturer
Won't boot-up disk	Disk/SMPTE Mux Prob.	Check ICs 126,127
Won't boot-up disk	No 1K pullup IC127 pin 2	Add pullup resistor
Won't load disks	Drive out of alignment or bad disk	Try different disks
Won't load disks	Drive out of alignment	Replace or align drive
Intermittant lock up	Intermittant CPU	Replace CPU
LCD reads Insert Disk	Faulty power to Disk	Check Disk power
LCD -> Loading Software	Disk data cable backwards	Install cable correctly

<b>Sync</b> Bad SMPTE sync	1-shot out of tolerance	Check 1-shot window
Bad SMPTE sync	No back pnl to Jack Gnd	Restore ground path
, -		i teolore greana patri
Audio Problems Oscillations in Sample	Trimmer RT1 set exactly to 800	Re-trim to approx. 804
Channel 1or 2 missing Channel 1or 2 muted	Bad SSM Chip Bad Filter Cap	Replace bad Chip Replace bad Cap.
Channel missing	Check IC112 Demux	Replace as necessary
Channel crosstalk	7523 in IC97 socket	Replace with 7524
Channel crosstalk	Bad 4051 Demux	Replace as necessary
Crackling Ch 1 and 2 or crosstalk	Bad IC 62 CS PAL	Replace bad Chip
Hiss or crackling channel	Bad Sample/Hold Cap.	Replace Cap.
Poor audio quality	DAC needs trim	Trim DAC etc.
Poor audio quality due to missing DAC bits	Bad IC151 or IC152	Replace bad chips
Metallic distortion when sounds are tuned	May be normal due to the way SP1200 tunes sounds	Explain facts to customer
Clank,Clunk, mult. sounds	Microcontroller problem	Look for bad levels $\mu C$
<b>Other</b> VU stuck high in sample mode	Offset in Anti-Alias Filter	Replace Op-amp or bad Componant
Slider doesn't work	Broken solder joint at pot	Resolder pot
Scratchy Pot	DC offset in circuit or bad pot	Clean pot or find offset
LCD Backlight intermittant		

### THEORY OF OPERATION

#### **OVERVIEW**

The SP1200 is very much like the Drumulator and the SP-12 in that it uses multiplexed audio controlled by a custom designed microcontroller and uses a Z-80 CPU. There are some major differences like the 12 bit format, disk drive and user sampling. Knowledge of the Drumulator and or SP-12 will be helpful in learning how the SP1200 functions.

The simplified block diagram (see fig 2) shows the entire SP1200. Starting at the top left we see that the sliders are read by an ADC circuit. The value is read from the data bus by the Z-80A when it selects the ADC chip.

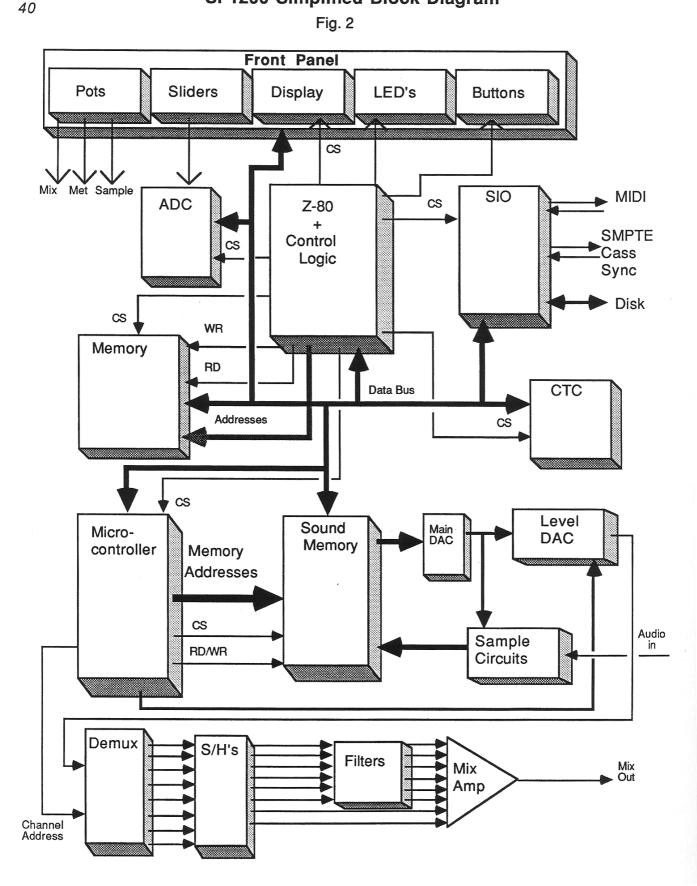
The LEDs are treated as a write only port. They are connected to a latch which the Z-80A writes to when an LED needs to be turned on or off.

The display is connected to the data bus and treated as a read/write port. All information for the user is written to this port in ASCII except for a few graphic symbols.

The pots are regular analog controls. The mix out pot is connected in the feedback loop of the mix out buffer amp. The metronome pot is connected from the metronome output to ground. The wiper is then summed into the mix out with the rest of the output channels. The sample gain pot has one end grounded and the other connected to the sample input jack. The wiper of the pot feeds the input buffer amp.

The buttons are set up in a matrix and decoded to determine which button was pressed. Two I/O ports are used for this. The first port is the decoder which the Z-80A writes to for row selection. The second port is used to read all the columns to determine which switch was pressed on the decoded row.

The Z-80A is the main CPU that runs the machine. It reads the buttons and sliders and writes to the display. I communicates to the world through the SIO (Serial Input Output). The instructions that boot the machine are contained in EPROM. The main operating instructions are loaded into RAM from the floppy disk on power up. This RAM called the Program Memory also contains the program variables, CPU stack and sequencer memory. The CTC is used



primarily for generating timed interrupts. The CPU is interrupted by the CTC to scan the buttons every 1.2 milliseconds. It also is used for sequencer timing and SMPTE/SYNC input and output timing. The microcontroller handles all the sound output control. It generates the memory timing and control signals as well as the memory addresses. It also generates the signals for the sound level control registers and timing for the de-multiplexing of sounds.

The sound memory is composed entirely of 4464 Dynamic RAMs which are four bits wide by 64K for a total sound memory size of 256K words. The sound memory is divided up into 4 banks of 2.5 seconds each. Sounds cannot cross over into another bank. Since the dynamic RAMs lose their memory when power is removed, any sound data that has not been saved to disk will be lost *forever*.

The DAC is a standard 12 bit linear device. It is used both for playing and sampling sounds.

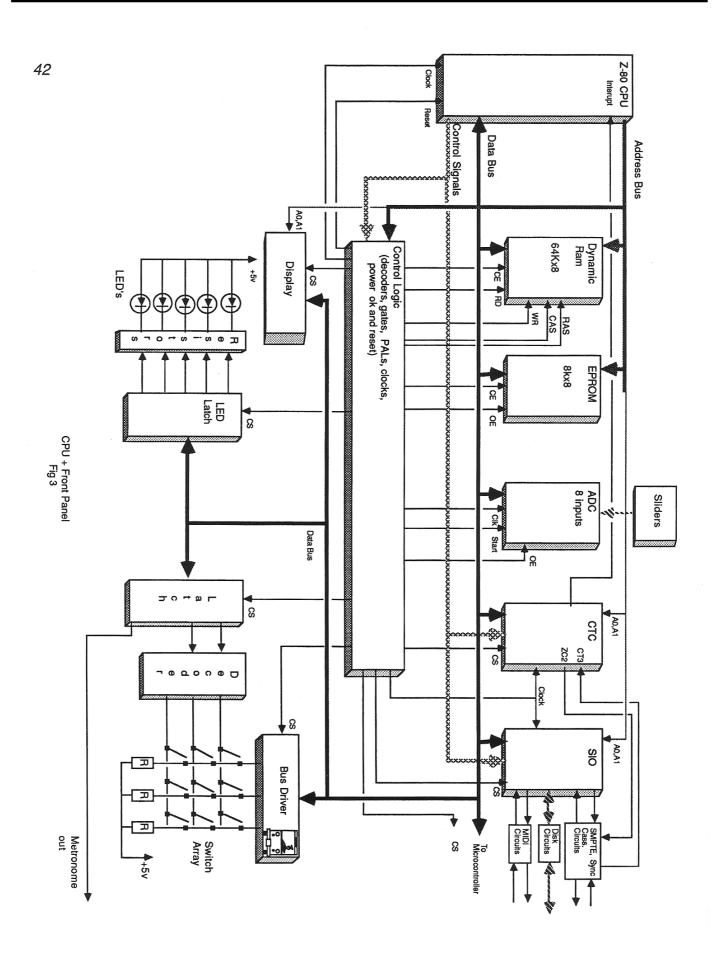
For signal level control a standard 8 bit multiplying DAC is used as an attenuator the signal being fed into the DAC reference. The level value is stored in a register in the microcontroller. It is sent to the level DAC at the appropriate time to control the level of each sound separately.

The sample circuit uses the 12 bit sound DAC and a successive approximation register to digitize the incoming signal. This is done under CPU control.

The de-multiplexer separates the 8 channels then routes them to the sample/holds. Two channels (7,8) are direct outs. The rest of the channels are filtered. The channels are summed together at the mix out amp. There are 8 separate outputs independent from the mix out out not shown in this diagram.

The SP1200 was designed to use 74HCT series logic instead of 74LS. We did this to lower the power requirements and use a smaller power supply. We do NOT recommend using 74LS chips as replacements for HCT as they overtax the power supply. There are some locations where LS is used because of circuit loading, however the majority of TTLICs are HCT.

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#### THE CPU AND FRONT PANEL

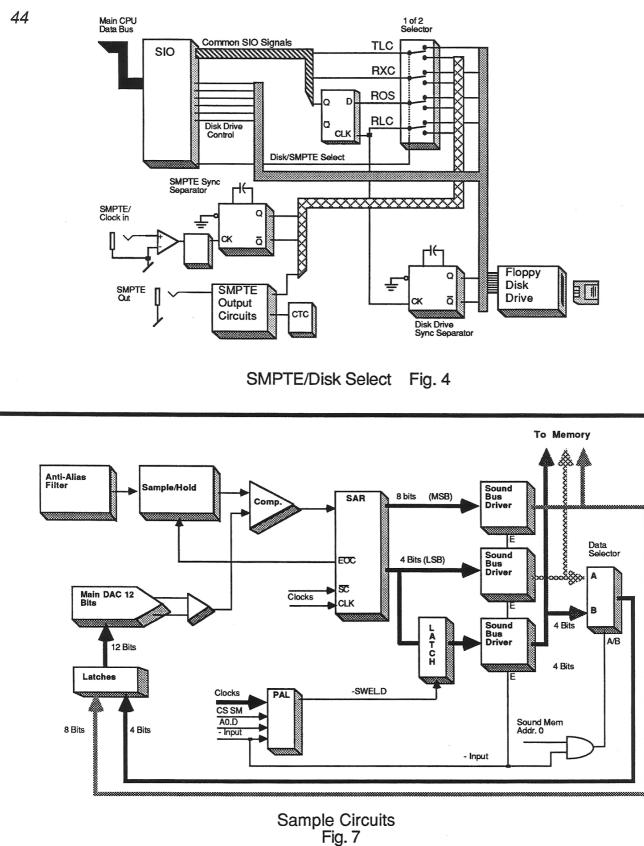
The SP1200 uses a Z-80A processor running at 3.3 mHz. Its memory consists of 8K bytes of EPROM memory and 64K of dynamic RAM. A PAL is used to decode the CPUs memory.

The pot ADC is a single chip. It has 8 analog inputs, 3 digital select lines to decode 1 of the 8 inputs, a clock input, a start conversion input, an end of conversion output and an output enable. The ADC is mapped into two of the Z-80As I/O ports. The first port written to select the 1 of 8 sliders and start the conversion. The second port is used to read back the digital value of the pot. Slider 8 is multiplexed with the dynamic button circuit on the front panel using a 4053 analog mux. The ADC reads the output of this circuit and sends it to the CPU to control the playback level.

The CTC (Counter Timer Circuit) is used primarily for interrupt driven timing functions in the software. The most often used timing function is for what we call housekeeping. This is an interrupt generated by the CTC every 1.2 milliseconds that reminds the CPU to read the front panel buttons and sliders. The second most often used CTC function is running the sequencer. If you look at schematic page 2 of 18 you will see that ZC2 (Zero Count channel 2) is connected to CT1 (Clock Trigger channel 1). This is done to cascade the two counters to provide very high resolution (.1 BPM) sequencer timing. The CTC is also used to generate a clock for the bit rate on the SMPTE/SYNC input. Lastly the CTC provides a transmit clock to the SIO (Serial Input/Output) for outputting SMPTE and click signals.

The SIO (Serial Input/Output) is used for all serial interfacing. It sends and receives all the signals for MIDI, SMPTE, Sync and the disk drive. As mentioned above, the CTC supplies the SIO with a clock for signal rate control of SMPTE. Channel A is dedicated to MIDI and the floppy disk drive, with conventional MIDI input, output and thru circuitry. Channel B is dedicated to the SMPTE/SYNC interface. The remaining pins on the SIO used for implementing part of the floppy disk drive interface.

The floppy disk drive actually uses both halves of the SIO. When the disk drive is in use, the TLC, RXC, ROS, and the RLC signals going to the lower half of the SIO are switched (by IC126) from the SMPTE decoders to the floppy disk circuits. Refer to the block diagram fig. 4. Since no other SP1200 functions are accessible during disk operations anyway, this works out fine.



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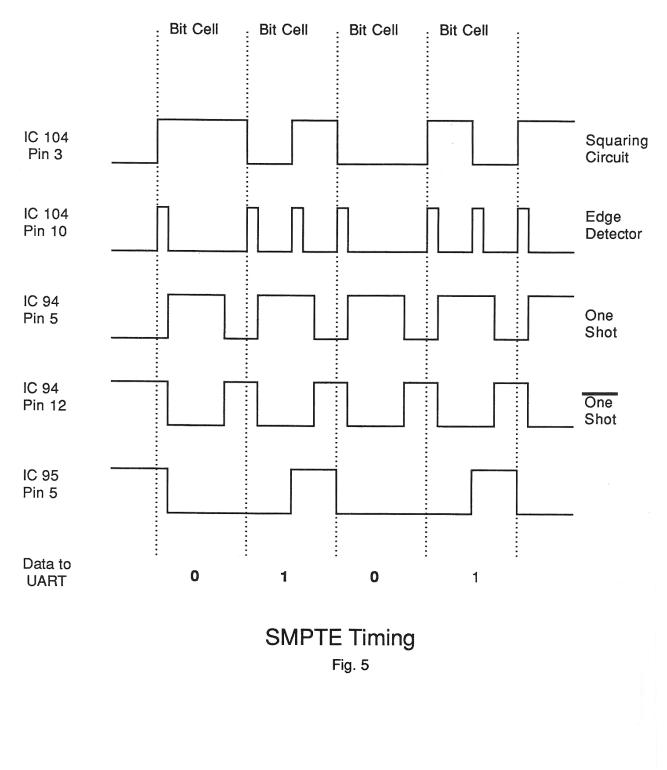
The SMPTE bi-phase decoder has two rates selected by the SIODTRB bit. Referring to the schematic, page 2 of 18, pin 25 of the SIO is connected to Q1 through R31. When pin 25 is high, Q1 is off. This causes IC 94's output pulse width to be determined by R41 and C81. When SIO pin 25 is low, Q1 is turned on which causes R37 to be in parallel with R41. This changes the RC time constant on IC94 which narrows the pulse on its output. This is done to accommodate the two SMPTE rates of 25 and 30 frames-per-second. Note: 24 and 25 frames-per-second are close enough to use the same size window. The input circuit is an LM 311 comparator which accommodates signals from approximately 250mV to 5 volts. Following this circuit is an edge detector. This generates a 25µS pulse on the rising or falling edge of the square wave input. The output of this circuit feeds the 1-shot circuit whose pulse width is set by Q1 as previously explained. To better understand the SMPTE circuit see fig. 5, which is a timing diagram of the circuit on page 2 of 18. The top of the diagram shows the bit cell time. Notice that a transition during a bit cell time indicates a 1 whereas no change is a 0. This is the standard SMPTE encoding scheme. The transition is a flux change on the tape. The signal recorded onto the tape is a square wave with two frequencies. One frequency is twice the rate of the other during a bit cell time. This is called bi-phase encoding. The higher frequency will cause a transition during a bit cell while the lower frequency will not. The top trace is the signal that came off the tape after it has been cleaned up by IC 104. Compare this to the data at the SIO and you can see how the flux changes correspond to the data. The second trace is the output of the edge detector circuit. It can be seen that this circuit puts out a pulse the width determined by R72 and C107, for every transition of the input signal. This signal is used to drive the 1 shot (IC94) and clock the flip-flop (IC95) to qualify the data. If the edge detector output is high during the middle of a bit cell time, it clocks the 1 shot data into it. This is decoding a 1. If there is not an edge detected during the bit cell then the flip-flop does not get clocked during the bit cell time and the output is a 0.

The LEDs are mapped into the CPU's I/O space as a write only port. The LED latch is connected directly to the data bus. The CPU writes a 0 to the latch to turn the LED on and a 1 to turn it off. The resistors prevent excessive current flow through the LEDs.

The display is connected directly to the data bus and is mapped as an I/O port. After the display is initialized, the CPU sends ASCII characters to it for displaying user messages.

The buttons are arranged in a matrix as can be seen in fig. 3. The

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buttons are also mapped in the CPUs I/O space. When the Z-80A wants to read the buttons it writes to the button latch which drives a decoder which selects a row. The decoder's output goes low for the selected row. The columns are pulled up with resistors. If a switch was pressed in the selected row the column line would be pulled low and the decoder would sink the current. The CPU then reads the I/O port which selects the button bus driver. If any output of the button bus driver is low then the button on that column (and the previously decoded row) is being pressed which will be read by the CPU.

#### MEMORY DE-MULTIPLEXING

The SP1200 uses 12 bit linear encoding for the sound data. To make the SP1200s design compatible with the SP-12, the memory was set up in the same way. Refer to Figure 6 for a block diagram of the memory de-multiplexing scheme. On the SP-12, the memory was Static RAM. Each RAM chip was 8 bits wide and so the 12 bit data was split up into a byte and a nibble. The SP1200 uses Dynamic RAMs which are 4 bits wide so that the memory organization seems unnecessarily complex. (Why not just use 3 RAMs per word?) Keep in mind that this is a carry over from the SP-12 and it all makes more sense. Sound memory address 0 switches the source of the low order nibble every other word. LSB RAMs A and B are alternately switched by a 1 of 2 data selector (IC 90). All addressing, de-multiplexing, RAS/CAS, etc. is controlled by the microcontroller and a couple of PALs (Programmable Logic Array) which is in turn controlled by the CPU. The CPU can read or write memory through the bi-directional data latches IC70 and IC71.

#### SAMPLING

The block diagram of the sampling circuits can be seen in fig. 7. The SP1200 uses the successive approximation technique to digitize the incoming audio signal.

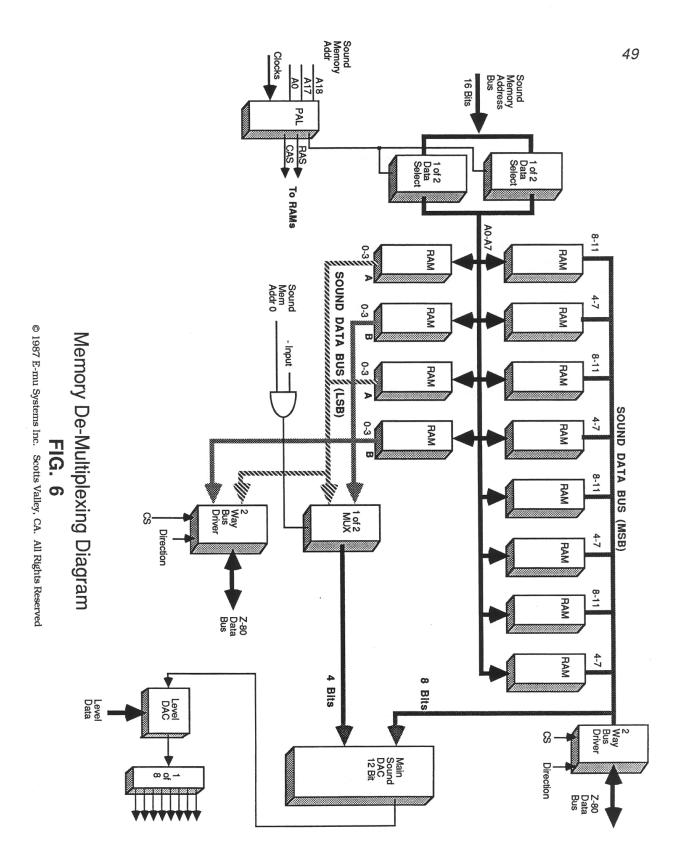
Before we get into the way the SP1200 samples, a basic explanation of successive approximation is in order. Referring to fig. 8 the three most basic elements of an 8 bit system can be seen. A few details such as the CPU and the sample/hold were left out in order to simplify the drawing. To start the process, the timer would send a start conversion signal and the successive approximation would begin. The SAR starts by setting bit 7 and looking at the output of the comparator. The output of the comparator tells the SAR whether the DAC's output is higher or lower than the input signal. If the DAC output is higher, the

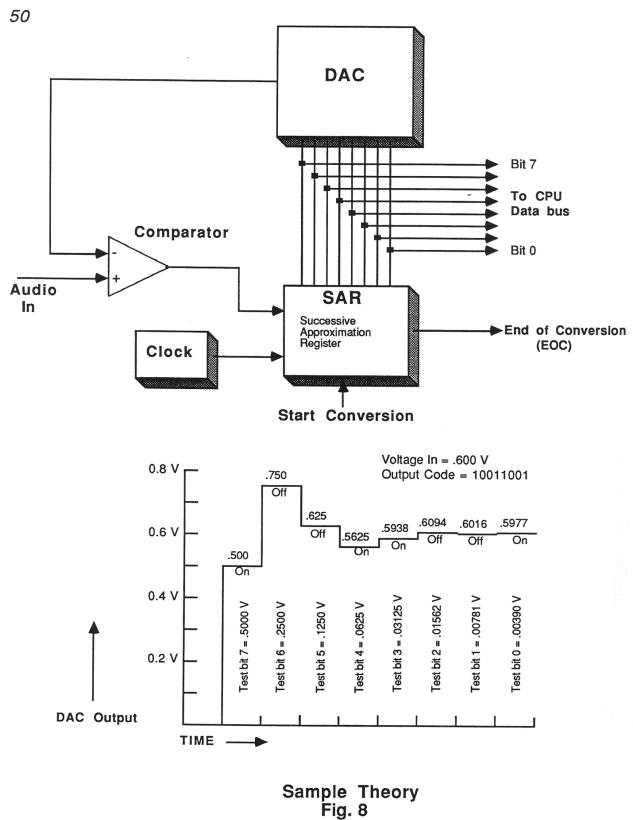
input bit will be set to 0. If the DAC output is lower, the input bit will be set to a 1. In fig. 8 the SAR set bit 7 which represents .500 volts and tested the comparator output. Since the + input was .600 V and the - was .500 V, the comparator's output was high which says the DAC is less than the input. The SAR will now set bit 7 high for the remainder of the test. As can be seen at the bottom of fig. 5, each bit is exactly half of the previous one. When the SAR sets bit 6 high, the DAC's output is the sum of bit 7 and bit 6 or .750 V. This is higher than the .600 V on the input and so the comparator output will be 0. Bit 6 is reset to 0. This process continues until all 8 bits are tested and set to 0 or 1. After all the bits are tested, the End of Conversion (EOC) line goes low to signal the main CPU that the data is ready to be stored in memory.

OK, back to the SP1200. Fig. 7 shows the basic blocks of the A/D converter. Starting from the left is the anti-aliasing filter. Aliasing is the phenomenon where the input frequency and the sample rate beat together to generate unwanted frequencies. These frequencies are the difference between the sample rate and the incoming signal. This happens when the input signal to be sampled exceeds half the sample rate and is allowed to be sampled. The anti-alias filter keeps this from happening. These filters usually have a very steep cutoff on the order of 42dB per octave and a cutoff frequency of less than half the sample rate of the system. Refer to schematic page 7 of 18 to see the anti-alias filter.

Next we have the sample/hold. This keeps the signal to be sampled steady while we convert it. At each End of Conversion signal, a new sample is held at the S/H. The comparator is used to compare the signal with the DAC output. The SAR sets and tests each bit using the DAC and comparator to determine the actual voltage of the input signal.The number of conversions made per second is the sample rate.

The next part of the circuit is a bit tricky. During sampling the - Input line is held low which selects only the "A" half of the data selector (IC 90). This allows the DAC free access to the data coming from the SAR. As was previously mentioned, the sound memory in the SP1200 is set up as if the data path were 16 bits wide (as it is in the SP-12). When a sound is sampled, the least significant 4 bits of each 12 bit word are only written to memory every other sample. Notice the split in the data path for the low nibble coming out of the SAR in fig. 7. A latch is used to hold the intermediate nibble until the next conversion. At that time the last nibble and the current nibble are both written into RAM at the same time. During the conversion process the CPU is in a wait state. Before the next conversion starts the PAL (IC69) removes the





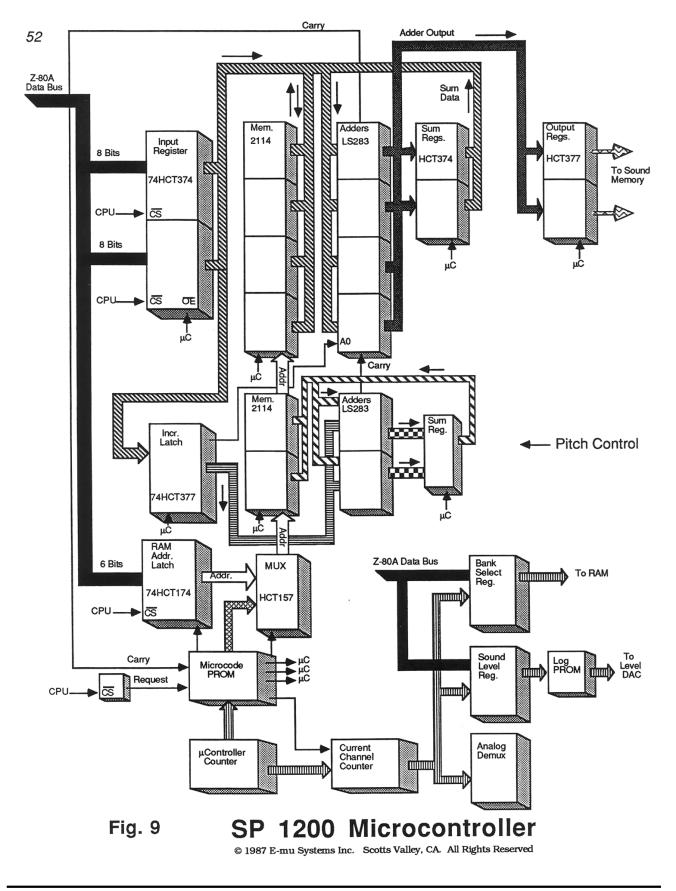
wait state and the data is written into RAM with the address provided by the CPU. The PAL decodes the -Input and -WR lines so that in actuality the CPU is *reading* the data in through IC 70 and 71 <u>while</u> RAM is being written so that it can update the display VU meter.

### THE MICROCONTROLLER

The Microcontroller ( $\mu$ C) is in control of playing the sounds. The CPU tells it where the sound is, the length, pitch, and loop points if any, then the  $\mu$ C generates all the signals to get the sound out of memory and to the DAC and sample/hold. As previously mentioned, the sound the SP1200 uses multiplexed audio. The  $\mu$ C de-multiplexes the signal using a 4051 and sample/holds it using caps and bi-FET op amps (see the schematic page 15 of 18). The  $\mu$ C (see fig. 9) is a special purpose dedicated microprocessor. It is not programmable so we call it a microcontroller. It generates all of the memory control signals and handles all the addressing during playback. It also controls the level of the sound being played using the level registers and has a bank select register for addressing memory beyond the 16 bits of the address latch output.

The Z-80A interfaces to the  $\mu$ C in 5 places. The first is the register file input latch. This is where the CPU writes the address, sound file size, pitch and any loop point data. The second interface is the register file RAM address latch. The CPU uses this latch to load register file RAM addresses. The third is the sound level register. This register holds the data that corresponds to the sound's playback level (see schematic page 8 of 18). Also on this page of the schematic is the fourth interface which is the bank select register. This is used to select which 64K byte block of memory will be accessed. The fifth interface is the request latch. This is set after the CPU has loaded data in the register file input latch and the register file RAM address latch. When the  $\mu$ C reads the request latch, it knows that data is in the file latches and writes it into the register file RAM. The data comes right of the Z-80A data bus. The CPU writes to the  $\mu$ Controller as 5 separate I/O ports.

To play a sound the CPU writes the Start Address, the Sound Length and the Pitch of the sound into the Input Registers (See Fig. 8). It also writes the Bank Number and the Sound Level into their registers. The  $\mu$ Controller takes over from here. With no pitch shifting, (as implemented on the Drumulator) the carry line entering the upper four adders is always 1 (A0 on the lower adder is 0). The Start and Size numbers get stored in the 2114 memory chips. Their locations in the 2114s correspond to the output channel number which is



controlled by the CPU via the RAM address latch. The microcode PROM controls the timing of all the registers and shifts the numbers through. Every time the address gets shifted through the adder, it is incremented by 1 and then sent to the output register and also back to the 2114 memories to await its next cycle through the adder. The Size number gets shifted through in the same way and signals the microcode PROM (via the carry out) that the sound has finished. OK, let's talk about pitch shifting. As previously mentioned, the Start, Size and Pitch numbers are stored in the upper 2114 memories. The Size number is incremented in the same way as with no pitch shift, but now the Carry In and A0 on the lower 2114 are not fixed. On each channel's cycle the appropriate pitch number is loaded into the Increment Latch. This number is added to the previous value in order to generate a carry value of either 0 or 1. A carry of 0 will cause the same sample to be played twice. A carry of 1 will increment the sample's address. If A0 is set to a 1 and the carry out of the lower adders is always 1, then the address will be incremented by 2. This will cause every other memory location to be skipped and the sound will play twice as fast or an octave higher. To shift down an octave, the A0 bit is set to 0 and the increment value is set so that the carry out of the lower adders will always be 0. Now every sample will play twice. It will take twice as long to play the sample and the pitch will be an octave lower. Intermediate pitch values (neither 0000000 or 1111111) will cause alternating 0 and 1 values at the carry out of the lower adders and either increment or not increment the current address value on that cycle. This will cause smaller pitch shift intervals. The CPU only sends values to the  $\mu$ Controller pitch register which create semitone tuning intervals.

#### POWER SUPPLY

The SP1200 uses a linear power supply to generate all the necessary voltages. The transformer, power switch, 115/220 switch, fuse and diode bridge are mounted on the back panel. The transformer has two secondaries. The lower secondary is a 36 volt AC center tap which is rectified by D3 through D6, filtered by C85 and C77 and regulated to +/- 15 volts by VR1 and VR2. The other secondary is is 12 volts which is rectified by the diode bridge, filtered by C153 and regulated to 5 volts by the 3-terminal IC regulator VR4.

# SIGNAL NAMES

### SP1200 SIGNAL NAME DEFINITIONS

The signal names are comprised of:

(a) + or - specifying active high or low.

(b) An abbreviation of the signal function.

(c) An abbreviation of the signal type.

(d) The signal's destination and source page numbers.

There are three types of signals; **D**, **V** and **I**. **D** stands for digital, **V** stands for voltage or an analog signal and **I** stands for a current.

EXAMPLE:	(a)	(b)	(c)
	-	8 M	.D
	(Low)	8 mHz Clock	Digital

#### SP 1200 Signal Name List

Name	Source	Destination	Туре	Description
Name +A0.D +A1.D +A2.D +A3.D +A4.D +A5.D +A5.D +A6.D +A7.D +A6.D +A7.D +A10.D +A10.D +A12.D +A13.D +A14.D +A15.D +ADCEOO	1 1 1 1 1 1 1 1 1 1 1 1 1	Destination 2,3,6,8,13 2,3,6,8 3,4 3,4 3,4 3,4 3,4 3,4 3,4 3,4 3 3 3 3	Type       IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	Main CPU Addr Bus 0 Main CPU Addr Bus 1 Main CPU Addr Bus 1 Main CPU Addr Bus 2 Main CPU Addr Bus 3 Main CPU Addr Bus 4 Main CPU Addr Bus 5 Main CPU Addr Bus 6 Main CPU Addr Bus 7 Main CPU Addr Bus 7 Main CPU Addr Bus 8 Main CPU Addr Bus 11 Main CPU Addr Bus 11 Main CPU Addr Bus 12 Main CPU Addr Bus 13 Main CPU Addr Bus 13 Main CPU Addr Bus 14 Main CPU Addr Bus 15 ADC End of Conv.
+C20M.D +C2MHZ.[	1	3,4 2		20 MHz Clock 2 MHz Clock

Name So	ource	Destination	Туре	Description
+C3MHZ.D -C6MHZ +C7.D +CARRY.D -CLE.D +CNL7.D +CNL00.V +CNLS0.D +CNLS1.D +CNLS2.D -CNLS2.D -CNLSH0.V +CNLSH1.V +CNLSH4.V +CNLSH5.V +CNLSH5.V +CNLSH5.V +CNLSH5.V +CNLSH6.V +CNLSH6.V +CNLSH6.V +CNLSH7.V -CSCTC.D +CSPB.D +CSRADC.D -CSWAD.D -CSWAD.D -CSWLD.D -CSWLD.D -CSWLD.D -CSWLVL.D -CSWLVL.D -CSWPBL.D +D0.D +D1.D +D2.D +D3.D +D4.D +D5.D +D6.D	1 1 1 8 9 7 1 6 6 7 7 7 7 5 5 5 5 5 5 5 5 5 5 5 5 5 5	3,4,10 4,10 9 7 7 14 17 17 8 8,15 8,15 8,15 8,15 8,15 8,15 8 16 16 17 17 17 17 17 15 2 8 5 5 2 7 5 9 6 6 9 8 8 5 2,3,5,6,7,8,9 3,5,6,7,8,9 3,5,6	TTL TTL TTL TTL TTL TTL Ana. Volt. Ana. Volt. Ana. Volt. Ana. Volt. Ana. Volt. Ana. Volt. Ana. Volt. Ana. Volt. Ana. Volt. Ana. Volt. TTL TTL TTL TTL TTL TTL TTL TTL TTL TT	3 MHz Clock 6 MHZ Clock $\mu$ C Carry Interconnect $\mu$ C Carry Out Carry Latch Enable Channel 7 Clk (Smpl) Dyn. Filt Out Ch. 0 Dyn. Filt Out Ch. 1 Channel Addr 0 Channel Addr 2 + Channel Addr 2 - Channel Addr 2 - Channel 0 S/H out Channel 1 S/H out Channel 3 S/H out Channel 3 S/H out Channel 6 S/H out Channel 6 S/H out Channel 7 S/H out CTC Chip Select Display Chip Select Push Button Chip Sel. Read ADC Chip Select Read Push Button CS SIO Chip Select Sund RAM Chip Sel. Z80 Wr Reg. File CS Wr LED Latch 0 CS Wr LED Latch 1 CS Z80 $\mu$ C Hi Byte CS Wr LED Latch 1 CS Z80 $\mu$ C Lo Byte CS Wr Vol. Hi Chip Sel Wr Vol. Lo Chip Sel Wr Vol. Lo Chip Sel Wr Vol. Hi Chip Sel Wr Vol. Data Bus 0 Main CPU Data Bus 1 Main CPU Data Bus 3 Main CPU Data Bus 3 Main CPU Data Bus 4 Main CPU Data Bus 5 Main CPU Data Bus 6
+D7.D	1	2,3,5,6,8,9	TTL	Main CPU Data Bus 7

Name	Source	Destination	Туре	Description
+DAC0.D +DAC1.D +DAC2.D +DAC3.D +DAC4.D +DAC5.D +DAC6.D +DAC6.D +DAC7.D +DAC8.D +DAC9.D +DAC10.D +DAC10.D +DAC11.D -DOE.D +DAC0UT.V +GAIN1.D -GAIN2.D +IL7.D -ILE.D -INDEX -INPUT.D -INPUT.D -INPUT.D -INPUT.D -INPUT.D +LD1.D +LD2.D +LD3.D +LD4.D +LD5.D +LD5.D +LD5.D +LD5.D +LD5.D +LD6.D +LD7.D -MI.D -MREQ.D -NMI.D +PHI.D +RA0.D +RA3.D +RA4.D +RA5.D +RAMA0.D +RAMA1.D	12 12 12 12 12 12 12 12 12 12 12 12 12 1	$     \begin{array}{r}       15 \\$	다. 아. Vot Vot	Sound DAC Data 0 Sound DAC Data 1 Sound DAC Data 2 Sound DAC Data 3 Sound DAC Data 3 Sound DAC Data 4 Sound DAC Data 5 Sound DAC Data 6 Sound DAC Data 7 Sound DAC Data 7 Sound DAC Data 9 Sound DAC Data 10 Sound DAC Data 10 Sound DAC Data 11 µC Latch Out Enable Sound DAC Output Env/Gain Control Bit 1 Env/Gain Control Bit 2 Increment Latch Bit 7 Increment Latch Enab. Floppy Disk Index Sample Input Select CPU Interrupt Request CPU I/O Request Latch DAC Data Level Data Bit 0 Level Data Bit 1 Level Data Bit 2 Level Data Bit 3 Level Data Bit 3 Level Data Bit 5 Level Data Bit 5 Level Data Bit 7 Z-80 M1 Snd Mem Addr Ltch En Z-80 Non-Mask Int. Z-80 Clock Reg. File Addr Bit 0 Reg. File Addr Bit 1 Reg. File Addr Bit 3 Reg. File Addr Bit 4 Reg. File Addr Bit 5
+LD3.D +LD4.D +LD5.D +LD5.D +LD7.D -M1.D -MLE.D -MREQ.D -NMI.D +PHI.D +RA0.D +RA1.D +RA2.D +RA3.D +RA4.D +RA5.D +RAMA0.D	8 8 8 1 7 1  1 7 7 7 7 7 7 7 10	15 15 15 15 2,3,4 9 3 1 2 8,9 8,9 8,9 8,9 8,9 8,9 8,9 8,9 11		Level Data Bit 3 Level Data Bit 4 Level Data Bit 5 Level Data Bit 6 Level Data Bit 7 Z-80 M1 Snd Mem Addr Ltch E Z-80 Mem. Req. Z-80 Non-Mask Int. Z-80 Clock Reg. File Addr Bit 0 Reg. File Addr Bit 1 Reg. File Addr Bit 2 Reg. File Addr Bit 3 Reg. File Addr Bit 3 Reg. File Addr Bit 4 Reg. File Addr Bit 5

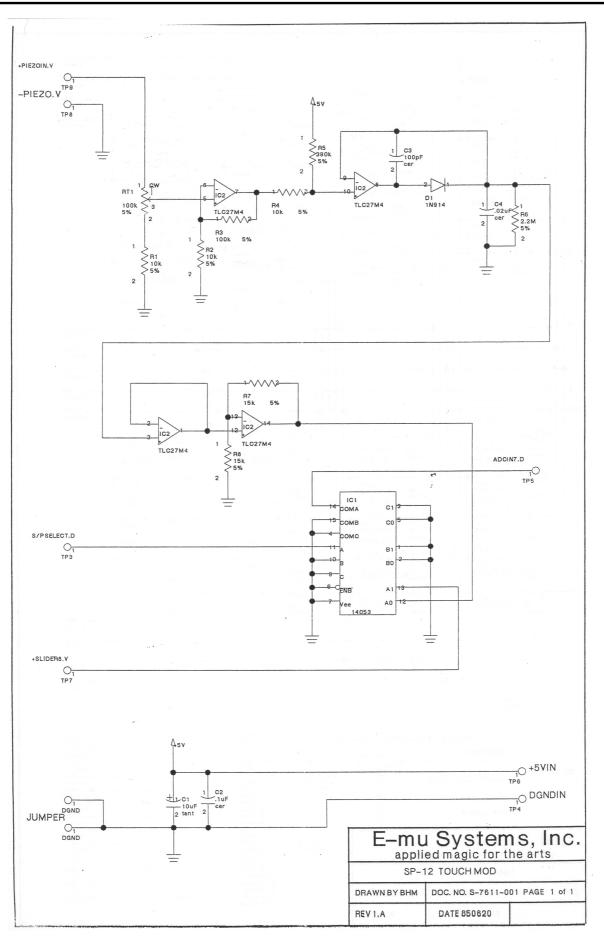
+RAMA2.D       10       11       TTL       RAM Addr Bit 2         +RAMA3.D       10       11       TTL       RAM Addr Bit 3         +RAMA4.D       10       11       TTL       RAM Addr Bit 4         +RAMA5.D       10       11       TTL       RAM Addr Bit 5         +RAMA6.D       10       11       TTL       RAM Addr Bit 6         +RAMA7.D       10       11       TTL       RAM Addr Bit 7         -RAS3.D       10       11       TTL       Row Addr. Strobe 3         -RAS5.D       10       11       TTL       Row Addr. Strobe 5         -RD.D       1       2,3,4       TTL       Z-80 Read         +RDB18.D       9       8       TTL       Reg. File Data Bit 16         +RDB18.D       9       8       TTL       Reg. File Data Bit 17         +RDB19.D       9       8       TTL       Reg. File Data Bit 17         +RDB23.D       9       8       TTL       Reg. File Data Bit 12         +RDB23.D       9       8       TTL       Reg. File Data Bit 12         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL <th>Name</th> <th>Source</th> <th>Destination</th> <th>Туре</th> <th>Description</th>	Name	Source	Destination	Туре	Description
+RAMA4.D       10       11       TTL       RAM Addr Bit 4         +RAMA5.D       10       11       TTL       RAM Addr Bit 5         +RAMA6.D       10       11       TTL       RAM Addr Bit 6         +RAMA6.D       10       11       TTL       RAM Addr Bit 7         -RAS3.D       10       11       TTL       Row Addr. Strobe 3         -RAS4.D       10       11       TTL       Row Addr. Strobe 4         -RAS5.D       10       11       TTL       Row Addr. Strobe 5         -RD.D       2,3,4       TTL       Reg. File Data Bit 16         +RDB16.D       9       8       TTL       Reg. File Data Bit 16         +RDB17.D       9       8       TTL       Reg. File Data Bit 16         +RDB19.D       9       8       TTL       Reg. File Data Bit 17         +RDB20.D       9       8       TTL       Reg. File Data Bit 18         +RDB20.D       9       8       TTL       Reg. File Data Bit 12         +RDB21.D       9       8       TTL       Reg. File Data Bit 21         +RDB23.D       9       8       TTL       Reg. File Data Bit 23         -RESET.D       1       3       TTL<					
+RAMA5.D       10       11       TTL       RAM Addr Bit 5         +RAMA6.D       10       11       TTL       RAM Addr Bit 6         +RAM7.D       10       11       TTL       RAM Addr Bit 7         -RAS3.D       10       11       TTL       Row Addr. Strobe 3         -RAS5.D       10       11       TTL       Row Addr. Strobe 4         -RAS5.D       10       11       TTL       Row Addr. Strobe 5         -RD.D       1       2,3,4       TTL       Reg. File Data Bit 16         +RDB17.D       9       8       TTL       Reg. File Data Bit 17         +RDB18.D       9       8       TTL       Reg. File Data Bit 120         +RDB20.D       9       8       TTL       Reg. File Data Bit 20         +RDB21.D       9       8       TTL       Reg. File Data Bit 21         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       1       3       TTL       Reg. File Data Bit 22         +RDB23.D       1 <td< td=""><td></td><td></td><td></td><td></td><td></td></td<>					
+RAMA6.D       10       11       TTL       RAM Addr Bit 6         +RAMA7.D       10       11       TTL       RAM Addr Bit 7         -RAS3.D       10       11       TTL       Row Addr. Strobe 3         -RAS4.D       10       11       TTL       Row Addr. Strobe 4         -RAS5.D       10       11       TTL       Row Addr. Strobe 5         -RD.D       1       2,3,4       TTL       Reg. File Data Bit 16         +RDB16.D       9       8       TTL       Reg. File Data Bit 17         +RDB18.D       9       8       TTL       Reg. File Data Bit 12         +RDB19.D       9       8       TTL       Reg. File Data Bit 20         +RDB20.D       9       8       TTL       Reg. File Data Bit 21         +RDB21.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 23         +RESET.D       1       2,3       TTL       Reset         -RFSH.D       1       3       TTL       Reset         -RFSPB.D       18       1       Heccive Clock       Refresh         +RWP.D       7       8,9       TTL					
+RAMA7.D       10       11       TTL       RAM Addr Bit 7         -RAS3.D       10       11       TTL       Row Addr. Strobe 3         -RAS4.D       10       11       TTL       Row Addr. Strobe 4         -RAS5.D       10       11       TTL       Row Addr. Strobe 5         -RD.D       1       2,3,4       TTL       Reg. File Data Bit 16         +RDB16.D       9       8       TTL       Reg. File Data Bit 16         +RDB17.D       9       8       TTL       Reg. File Data Bit 17         +RDB19.D       9       8       TTL       Reg. File Data Bit 16         +RDB20.D       9       8       TTL       Reg. File Data Bit 20         +RDB21.D       9       8       TTL       Reg. File Data Bit 21         +RDB22.D       9       8       TTL       Reg. File Data Bit 22         +RDB22.D       9       8       TTL       Reg. File Data Bit 23         -RESET.D       1       2,3       TTL       Reg. File Data Bit 23         -RESET.D       1       2,3       TTL       Receive Latch Clock         +ROS.D       4       2       TTL       Receive Clock         +RSTPB.D       18					
-RAS3.D       10       11       TTL       Row Addr. Strobe 3         -RAS5.D       10       11       TTL       Row Addr. Strobe 4         -RAS5.D       10       11       TTL       Row Addr. Strobe 5         -RD.D       1       2,3,4       TTL       Reg. File Data Bit 16         +RDB16.D       9       8       TTL       Reg. File Data Bit 17         +RDB17.D       9       8       TTL       Reg. File Data Bit 17         +RDB18.D       9       8       TTL       Reg. File Data Bit 17         +RDB17.D       9       8       TTL       Reg. File Data Bit 17         +RDB20.D       9       8       TTL       Reg. File Data Bit 21         +RDB21.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 23         -RESET.D       1       2,3       TTL       Reg. File Data Bit 23         -RFSH.D       1       3       TTL       Receive Clock         +RDS.D       4       2       TTL       Receive Clock         +RSTPB.D       18					
-RAS4.D       10       11       TTL       Row Addr. Strobe 4         -RAS5.D       10       11       TTL       Row Addr. Strobe 5         -RD.D       1       2,3,4       TTL       Z80 Read         +RDB16.D       9       8       TTL       Reg. File Data Bit 16         +RDB17.D       9       8       TTL       Reg. File Data Bit 17         +RDB18.D       9       8       TTL       Reg. File Data Bit 17         +RDB19.D       9       8       TTL       Reg. File Data Bit 19         +RDB20.D       9       8       TTL       Reg. File Data Bit 20         +RDB21.D       9       8       TTL       Reg. File Data Bit 21         +RDB22.D       9       8       TTL       Reg. File Data Bit 22         +RDB2.D       9       8       TTL       Reg. File Data Bit 22         +RDB2.D       1       3       TTL       Reg. File Data Bit 23         -RESET.D       1       2,3       TTL       Reset         +RFSH.D       1       3       TTL       Pynamic RAM Refresh         +RLC.D       4       2       TTL       Receive Clock         +RSB0.D       13       12       TTL <td></td> <td></td> <td></td> <td></td> <td></td>					
-RAS5.D       10       11       TTL       Row Addr. Strobe 5         -RD.D       1       2,3,4       TTL       Z80 Read         +RDB16.D       9       8       TTL       Reg. File Data Bit 16         +RDB17.D       9       8       TTL       Reg. File Data Bit 17         +RDB18.D       9       8       TTL       Reg. File Data Bit 17         +RDB19.D       9       8       TTL       Reg. File Data Bit 12         +RDB20.D       9       8       TTL       Reg. File Data Bit 20         +RDB21.D       9       8       TTL       Reg. File Data Bit 21         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 21         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 23         -RESET.D       1       2,3       TTL       Reset         -RFSH.D       1       3       TTL       Receive Cach Clock         +ROS.D       4       2       TTL       Receive Clock         +SDB0.D       13       12       TTL					
-RD.D       1       2,3,4       TTL       Z-80 Read         +RDB16.D       9       8       TTL       Reg. File Data Bit 16         +RDB17.D       9       8       TTL       Reg. File Data Bit 17         +RDB18.D       9       8       TTL       Reg. File Data Bit 17         +RDB19.D       9       8       TTL       Reg. File Data Bit 18         +RDB20.D       9       8       TTL       Reg. File Data Bit 20         +RDB21.D       9       8       TTL       Reg. File Data Bit 21         +RDB22.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 23         -RESET.D       1       2,3       TTL       Reset         -RFSH.D       1       3       TTL       Receive Latch Clock         +ROS.D       4       2       TTL       Receive Clock         +RWP.D       7       8,9       TTL       Reg. File Read/Write         +RSTPB.D       13       12       TTL       StO Receive Clock         +SDB0.D       10,11       12,13       TTL       Sto Receive Clock         +SDB1.D       13       12 <td< td=""><td></td><td></td><td></td><td></td><td></td></td<>					
+RDB16.D       9       8       TTL       Reg. File Data Bit 16         +RDB17.D       9       8       TTL       Reg. File Data Bit 17         +RDB18.D       9       8       TTL       Reg. File Data Bit 17         +RDB19.D       9       8       TTL       Reg. File Data Bit 18         +RDB20.D       9       8       TTL       Reg. File Data Bit 20         +RDB21.D       9       8       TTL       Reg. File Data Bit 21         +RDB22.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 23         -RESET.D       1       2,3       TTL       Reset         -RFSH.D       1       3       TTL       Reset         -RFSH.D       1       3       TTL       Receive Cone-Shot Clk         +RSDD       4       2       TTL       Receive Cone-Shot Clk         +RSTPB.D       18       1       TTL       SIO Receive Clock         +SDB0.D       10,11       12,13       TTL       SID Data Bit 0 (Demx)         +SDB0.D       10,11       12,13       TTL       SID Data Bus A Bit 0         +SDB1.D       13       12 </td <td></td> <td></td> <td></td> <td></td> <td></td>					
+RDB17.D       9       8       TTL       Reg. File Data Bit 17         +RDB18.D       9       8       TTL       Reg. File Data Bit 18         +RDB19.D       9       8       TTL       Reg. File Data Bit 19         +RDB20.D       9       8       TTL       Reg. File Data Bit 20         +RDB21.D       9       8       TTL       Reg. File Data Bit 21         +RDB22.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 23         -RESET.D       1       2,3       TTL       Reset         -RFSH.D       1       3       TTL       Pynamic RAM Refresh         +RLC.D       4       2       TTL       Receive Clock         +RSTPB.D       18       1       TTL       Reg. File Read/Write         +RXC.D       4       2       TTL       Snd Data Bus A Bit 0         +SDB0A.D       10,11       12,13					
+RDB18.D       9       8       TTL       Reg. File Data Bit 18         +RDB19.D       9       8       TTL       Reg. File Data Bit 19         +RDB20.D       9       8       TTL       Reg. File Data Bit 20         +RDB21.D       9       8       TTL       Reg. File Data Bit 21         +RDB22.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 23         -RESET.D       1       2,3       TTL       Reset         -RFSH.D       1       3       TTL       Receive Latch Clock         +ROS.D       4       2       TTL       Receive One-Shot Clk         -RSTPB.D       18       1       TTL       Receive Clock         +SDB0.D       13       12       TTL       Snd Data Bit 0 (Demx)         +SDB0.D       13       12       TTL       Snd Data Bus A Bit 0         +SDB0.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB0.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB0.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       10,11       12					
+RDB19.D       9       8       TTL       Reg. File Data Bit 19         +RDB20.D       9       8       TTL       Reg. File Data Bit 20         +RDB21.D       9       8       TTL       Reg. File Data Bit 21         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 22         +RDB20.D       1       2,3       TTL       Reset         -RESET.D       1       2,3       TTL       Reset         +RC.D       4       2       TTL       Receive Cone-Shot Clk         -RSTPB.D       18       1       TTL       Sho Data Bit 0 (Demx)         +SDB0.D       13       12       TTL       Shd Data Bus A Bit 0         +SDB0.D       10,11       12,13       TTL       Shd Data Bus A Bit 1         +SDB1.D       10,11			8		
+RDB20.D       9       8       TTL       Reg. File Data Bit 20         +RDB21.D       9       8       TTL       Reg. File Data Bit 21         +RDB22.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 23         -RESET.D       1       2,3       TTL       Reset         -RFSH.D       1       3       TTL       Receive Latch Clock         +ROS.D       4       2       TTL       Receive One-Shot Clk         +RSTPB.D       18       1       TTL       Force Reset Test Point         -RWC.D       7       8,9       TTL       SIO Receive Clock         +SDB0.D       13       12       TTL       SIO Receive Clock         +SDB0.D       13       12       TTL       SIO Receive Clock         +SDB0.D       10,11       12,13       TTL       Snd Data Bus A Bit 0         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB3.D       10,11 <t< td=""><td></td><td></td><td>8</td><td></td><td></td></t<>			8		
+RDB21.D       9       8       TTL       Reg. File Data Bit 21         +RDB22.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 23         -RESET.D       1       2,3       TTL       Reset         -RFSH.D       1       3       TTL       Dynamic RAM Refresh         +RC.D       4       2       TTL       Receive Latch Clock         +RSTPB.D       18       1       TTL       Force Reset Test Point         -RWP.D       7       8,9       TTL       SIO Receive Clock         +SDB0.D       13       12       TTL       SIO Receive Clock         +SDB0A.D       10,11       12,13       TTL       Snd Data Bus A Bit 0         +SDB0B.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB3.D       10,11			8		
+RDB22.D       9       8       TTL       Reg. File Data Bit 22         +RDB23.D       9       8       TTL       Reg. File Data Bit 23         -RESET.D       1       2,3       TTL       Reset         -RFSH.D       1       3       TTL       Dynamic RAM Refresh         +RLC.D       4       2       TTL       Receive Latch Clock         +ROS.D       4       2       TTL       Receive One-Shot Clk         -RSTPB.D       18       1       TTL       Force Reset Test Point         -RWP.D       7       8,9       TTL       SIO Receive Clock         +SDB0.D       13       12       TTL       Snd Data Bit 0 (Demx)         +SDB0A.D       10,11       12,13       TTL       Snd Data Bus A Bit 0         +SDB0A.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB3.D       10,11       12,13       TTL       Snd Data Bus A Bit 2         +SDB2.D			8		
+RDB23.D       9       8       TTL       Reg. File Data Bit 23         -RESET.D       1       2,3       TTL       Reset         -RFSH.D       1       3       TTL       Dynamic RAM Refresh         +RLC.D       4       2       TTL       Receive Latch Clock         +ROS.D       4       2       TTL       Receive One-Shot Clk         -RSTPB.D       18       1       TTL       Force Reset Test Point         -RWP.D       7       8,9       TTL       Reg. File Read/Write         +RXC.D       4       2       TTL       SIO Receive Clock         +SDB0.D       13       12       TTL       Snd Data Bus A Bit 0         +SDB0A.D       10,11       12,13       TTL       Snd Data Bus A Bit 0         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB2.D       13       12       TTL       Snd Data Bus A Bit 2         +SDB2.D       13       12       TTL       Snd Data Bus A Bit 2         +SDB3.D       10,11			8		
-RESET.D       1       2,3       TTL       Reset         -RFSH.D       1       3       TTL       Dynamic RAM Refresh         +RLC.D       4       2       TTL       Receive Latch Clock         +ROS.D       4       2       TTL       Receive Latch Clock         +ROS.D       4       2       TTL       Receive One-Shot Clk         -RSTPB.D       18       1       TTL       Force Reset Test Point         -RWP.D       7       8,9       TTL       Reg. File Read/Write         +RXC.D       4       2       TTL       SIO Receive Clock         +SDB0.D       13       12       TTL       Snd Data Bus A Bit 0         +SDB0A.D       10,11       12,13       TTL       Snd Data Bus A Bit 0         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB2.D       13       12       TTL       Snd Data Bus A Bit 2         +SDB3.D       10,11       12,13       TTL       Snd Data Bus A Bit 2         +SDB3.D       13			8		-
-RFSH.D       1       3       TTL       Dynamic RAM Refresh         +RLC.D       4       2       TTL       Receive Latch Clock         +ROS.D       4       2       TTL       Receive One-Shot Clk         -RSTPB.D       18       1       TTL       Receive One-Shot Clk         -RSTPB.D       7       8,9       TTL       Receive One-Shot Clk         +RXC.D       4       2       TTL       SIO Receive Clock         +SDB0.D       13       12       TTL       SIO Receive Clock         +SDB0A.D       10,11       12,13       TTL       Snd Data Bus A Bit 0         +SDB0B.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB1.D       10,11       12,13       TTL       Snd Data Bus A Bit 2         +SDB2.D       13       12       TTL       Snd Data Bus A Bit 2         +SDB2.D       10,11       12,13       TTL       Snd Data Bus A Bit 2         +SDB3.					
+RLC.D       4       2       TTL       Receive Latch Clock         +ROS.D       4       2       TTL       Receive One-Shot Clk         -RSTPB.D       18       1       TTL       Force Reset Test Point         -RWP.D       7       8,9       TTL       Reg. File Read/Write         +RXC.D       4       2       TTL       SIO Receive Clock         +SDB0.D       13       12       TTL       Snd Data Bit 0 (Demx)         +SDB0A.D       10,11       12,13       TTL       Snd Data Bus A Bit 0         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 0         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB2.D       10,11       12,13       TTL       Snd Data Bus A Bit 2         +SDB2.D       10,11       12,13       TTL       Snd Data Bus A Bit 2         +SDB3.D       10,11       12,13       TTL       Snd Data Bus B Bit 3					
-RSTPB.D       18       1       TTL       Force Reset Test Point         -RWP.D       7       8,9       TTL       Reg. File Read/Write         +RXC.D       4       2       TTL       SIO Receive Clock         +SDB0.D       13       12       TTL       Snd Data Bit 0 (Demx)         +SDB0A.D       10,11       12,13       TTL       Snd Data Bus A Bit 0         +SDB0B.D       10,11       12,13       TTL       Snd Data Bus A Bit 0         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 0         +SDB1.D       13,12       TTL       Snd Data Bus A Bit 1         +SDB1.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB1.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB2.D       13       12       TTL       Snd Data Bus A Bit 2         +SDB2.D       10,11       12,13       TTL       Snd Data Bus A Bit 2         +SDB3.D       10,11       12,13       TTL       Snd Data Bus A Bit 3         +SDB3.D       10,11       12,13       TTL       Snd Data Bus A Bit 3         +SDB3.D       10,11       12,13       TTL       Snd Data Bus Bit 3	+RLC.D	4	2	TTL	Receive Latch Clock
-RWP.D       7       8,9       TTL       Reg. File Read/Write         +RXC.D       4       2       TTL       SIO Receive Clock         +SDB0.D       13       12       TTL       Snd Data Bit 0 (Demx)         +SDB0A.D       10,11       12,13       TTL       Snd Data Bus A Bit 0         +SDB0B.D       10,11       12,13       TTL       Snd Data Bus A Bit 0         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 0         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB1A.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB2.D       13       12       TTL       Snd Data Bus A Bit 2         +SDB2.D       10,11       12,13       TTL       Snd Data Bus A Bit 2         +SDB3.D       10,11       12,13       TTL       Snd Data Bus A Bit 3         +SDB3.D       10,11       12,13       TTL       Snd Data Bus A Bit 3         +SDB3.D       10,11       12,13       TTL       Snd Data Bus Bit 4 </td <td>+ROS.D</td> <td>4</td> <td></td> <td>TTL</td> <td>Receive One-Shot Clk</td>	+ROS.D	4		TTL	Receive One-Shot Clk
+RXC.D       4       2       TTL       SIO Receive Clock         +SDB0.D       13       12       TTL       Snd Data Bit 0 (Demx)         +SDB0A.D       10,11       12,13       TTL       Snd Data Bus A Bit 0         +SDB0B.D       10,11       12,13       TTL       Snd Data Bus A Bit 0         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB1.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB1B.D       10,11       12,13       TTL       Snd Data Bus A Bit 1         +SDB2.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB2.D       13       12       TTL       Snd Data Bus A Bit 1         +SDB2.D       13       12       TTL       Snd Data Bus A Bit 2         +SDB2.D       10,11       12,13       TTL       Snd Data Bus A Bit 2         +SDB3.D       10,11       12,13       TTL       Snd Data Bus A Bit 3         +SDB3.D       10,11       12,13       TTL       Snd Data Bus A Bit 3         +SDB3.D       10,11       12,13       TTL       Snd Data Bus B Bit 3	-RSTPB.D	0 18	1	TTL	
+SDB0.D1312TTLSnd Data Bit 0 (Demx)+SDB0A.D10,1112,13TTLSnd Data Bus A Bit 0+SDB0B.D10,1112,13TTLSnd Data Bus B Bit 0+SDB1.D1312TTLSnd Data Bus A Bit 1 (A+B)+SDB1A.D10,1112,13TTLSnd Data Bus A Bit 1+SDB1B.D10,1112,13TTLSnd Data Bus A Bit 1+SDB1B.D10,1112,13TTLSnd Data Bus A Bit 2 (A+B)+SDB2.D1312TTLSnd Data Bus A Bit 2+SDB2A.D10,1112,13TTLSnd Data Bus B Bit 2+SDB3.D10,1112,13TTLSnd Data Bus A Bit 3 (A+B)+SDB3A.D10,1112,13TTLSnd Data Bus A Bit 3+SDB3B.D10,1112,13TTLSnd Data Bus B Bit 3+SDB4.D10,1112,13TTLSnd Data Bus B Bit 3+SDB5.D10,1112,13TTLSnd Data Bus B Bit 3+SDB5.D10,1112,13TTLSnd Data Bus B Bit 3+SDB5.D10,1112,13TTLSnd Data Bus Bit 4+SDB7.D10,1112,13TTLSnd Data Bus Bit 6+SDB7.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 8		7			
+SDB0A.D10,1112,13TTLSnd Data Bus A Bit 0+SDB0B.D10,1112,13TTLSnd Data Bus B Bit 0+SDB1.D1312TTLSnd Data Bus A Bit 1 (A+B)+SDB1A.D10,1112,13TTLSnd Data Bus A Bit 1+SDB1B.D10,1112,13TTLSnd Data Bus A Bit 1+SDB1B.D10,1112,13TTLSnd Data Bus B Bit 1+SDB2.D1312TTLSnd Data Bus B Bit 2 (A+B)+SDB2A.D10,1112,13TTLSnd Data Bus A Bit 2+SDB3.D10,1112,13TTLSnd Data Bus A Bit 3 (A+B)+SDB3A.D10,1112,13TTLSnd Data Bus A Bit 3+SDB3B.D10,1112,13TTLSnd Data Bus B Bit 3+SDB4.D10,1112,13TTLSnd Data Bus B Bit 3+SDB5.D10,1112,13TTLSnd Data Bus Bit 4+SDB5.D10,1112,13TTLSnd Data Bus Bit 5+SDB6.D10,1112,13TTLSnd Data Bus Bit 6+SDB7.D10,1112,13TTLSnd Data Bus Bit 6+SDB7.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 8					
+SDB0B.D10,1112,13TTLSnd Data Bus B Bit 0+SDB1.D1312TTLSnd Data Bit 1 (A+B)+SDB1A.D10,1112,13TTLSnd Data Bus A Bit 1+SDB1B.D10,1112,13TTLSnd Data Bus B Bit 1+SDB2.D1312TTLSnd Data Bus A Bit 2 (A+B)+SDB2A.D10,1112,13TTLSnd Data Bus A Bit 2+SDB2B.D10,1112,13TTLSnd Data Bus B Bit 2+SDB3.D1312TTLSnd Data Bus A Bit 3 (A+B)+SDB3A.D10,1112,13TTLSnd Data Bus A Bit 3+SDB3B.D10,1112,13TTLSnd Data Bus B Bit 3+SDB4.D10,1112,13TTLSnd Data Bus B Bit 3+SDB5.D10,1112,13TTLSnd Data Bus Bit 4+SDB5.D10,1112,13TTLSnd Data Bus Bit 5+SDB6.D10,1112,13TTLSnd Data Bus Bit 6+SDB7.D10,1112,13TTLSnd Data Bus Bit 6+SDB8.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 7					
+SDB1.D1312TTLSnd Data Bit 1 (A+B)+SDB1A.D10,1112,13TTLSnd Data Bus A Bit 1+SDB1B.D10,1112,13TTLSnd Data Bus B Bit 1+SDB2.D1312TTLSnd Data Bus A Bit 2 (A+B)+SDB2A.D10,1112,13TTLSnd Data Bus A Bit 2+SDB2B.D10,1112,13TTLSnd Data Bus A Bit 2+SDB3.D10,1112,13TTLSnd Data Bus A Bit 3 (A+B)+SDB3A.D10,1112,13TTLSnd Data Bus A Bit 3+SDB3B.D10,1112,13TTLSnd Data Bus B Bit 3+SDB4.D10,1112,13TTLSnd Data Bus B Bit 3+SDB5.D10,1112,13TTLSnd Data Bus Bit 4+SDB5.D10,1112,13TTLSnd Data Bus Bit 5+SDB7.D10,1112,13TTLSnd Data Bus Bit 6+SDB8.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 7					
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+SDB1B.D10,1112,13TTLSnd Data Bus B Bit 1+SDB2.D1312TTLSnd Data Bit 2 (A+B)+SDB2A.D10,1112,13TTLSnd Data Bus A Bit 2+SDB2B.D10,1112,13TTLSnd Data Bus B Bit 2+SDB3.D1312TTLSnd Data Bus A Bit 3 (A+B)+SDB3A.D10,1112,13TTLSnd Data Bus A Bit 3+SDB3B.D10,1112,13TTLSnd Data Bus A Bit 3+SDB3B.D10,1112,13TTLSnd Data Bus B Bit 3+SDB4.D10,1112,13TTLSnd Data Bus B Bit 5+SDB6.D10,1112,13TTLSnd Data Bus Bit 5+SDB7.D10,1112,13TTLSnd Data Bus Bit 6+SDB8.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 8					
+SDB2.D1312TTLSnd Data Bit 2 (A+B)+SDB2A.D10,1112,13TTLSnd Data Bus A Bit 2+SDB2B.D10,1112,13TTLSnd Data Bus B Bit 2+SDB3.D1312TTLSnd Data Bus A Bit 3 (A+B)+SDB3A.D10,1112,13TTLSnd Data Bus A Bit 3+SDB3B.D10,1112,13TTLSnd Data Bus A Bit 3+SDB3B.D10,1112,13TTLSnd Data Bus B Bit 3+SDB4.D10,1112,13TTLSnd Data Bus Bit 4+SDB5.D10,1112,13TTLSnd Data Bus Bit 5+SDB6.D10,1112,13TTLSnd Data Bus Bit 6+SDB7.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 8		•			
+SDB2A.D10,1112,13TTLSnd Data Bus Å Bit 2+SDB2B.D10,1112,13TTLSnd Data Bus B Bit 2+SDB3.D1312TTLSnd Data Bit 3 (A+B)+SDB3A.D10,1112,13TTLSnd Data Bus A Bit 3+SDB3B.D10,1112,13TTLSnd Data Bus B Bit 3+SDB4.D10,1112,13TTLSnd Data Bus B Bit 3+SDB5.D10,1112,13TTLSnd Data Bus Bit 4+SDB6.D10,1112,13TTLSnd Data Bus Bit 5+SDB7.D10,1112,13TTLSnd Data Bus Bit 6+SDB8.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 7					
+SDB2B.D10,1112,13TTLSnd Data Bus B Bit 2+SDB3.D1312TTLSnd Data Bit 3 (A+B)+SDB3A.D10,1112,13TTLSnd Data Bus A Bit 3+SDB3B.D10,1112,13TTLSnd Data Bus B Bit 3+SDB4.D10,1112,13TTLSnd Data Bus B Bit 4+SDB5.D10,1112,13TTLSnd Data Bus Bit 5+SDB6.D10,1112,13TTLSnd Data Bus Bit 5+SDB7.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 7					
+SDB3.D1312TTLSnd Data Bit 3 (A+B)+SDB3A.D10,1112,13TTLSnd Data Bus A Bit 3+SDB3B.D10,1112,13TTLSnd Data Bus B Bit 3+SDB4.D10,1112,13TTLSnd Data Bus Bit 4+SDB5.D10,1112,13TTLSnd Data Bus Bit 5+SDB6.D10,1112,13TTLSnd Data Bus Bit 6+SDB7.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 7					
+SDB3A.D10,1112,13TTLSnd Data Bus A Bit 3+SDB3B.D10,1112,13TTLSnd Data Bus B Bit 3+SDB4.D10,1112,13TTLSnd Data Bus Bit 4+SDB5.D10,1112,13TTLSnd Data Bus Bit 5+SDB6.D10,1112,13TTLSnd Data Bus Bit 6+SDB7.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 7					
+SDB3B.D10,1112,13TTLSnd Data Bus B Bit 3+SDB4.D10,1112,13TTLSnd Data Bus Bit 4+SDB5.D10,1112,13TTLSnd Data Bus Bit 5+SDB6.D10,1112,13TTLSnd Data Bus Bit 6+SDB7.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 7					
+SDB4.D       10,11       12,13       TTL       Snd Data Bus Bit 4         +SDB5.D       10,11       12,13       TTL       Snd Data Bus Bit 5         +SDB6.D       10,11       12,13       TTL       Snd Data Bus Bit 6         +SDB7.D       10,11       12,13       TTL       Snd Data Bus Bit 7         +SDB8.D       10,11       12,13       TTL       Snd Data Bus Bit 7			12,13		
+SDB5.D10,1112,13TTLSnd Data Bus Bit 5+SDB6.D10,1112,13TTLSnd Data Bus Bit 6+SDB7.D10,1112,13TTLSnd Data Bus Bit 7+SDB8.D10,1112,13TTLSnd Data Bus Bit 8					
+SDB6.D         10,11         12,13         TTL         Snd Data Bus Bit 6           +SDB7.D         10,11         12,13         TTL         Snd Data Bus Bit 7           +SDB8.D         10,11         12,13         TTL         Snd Data Bus Bit 7					
+SDB7.D         10,11         12,13         TTL         Snd Data Bus Bit 7           +SDB8.D         10,11         12,13         TTL         Snd Data Bus Bit 8					
+SDB8.D 10,11 12,13 TTL Snd Data Bus Bit 8					
+SDB9.D 10,11 12,13 TTL Snd Data Bus Bit 9		•			Snd Data Bus Bit 9
+SDB10.D 10,11 12,13 TTL Snd Data Bus Bit 10		•			Snd Data Bus Bit 10

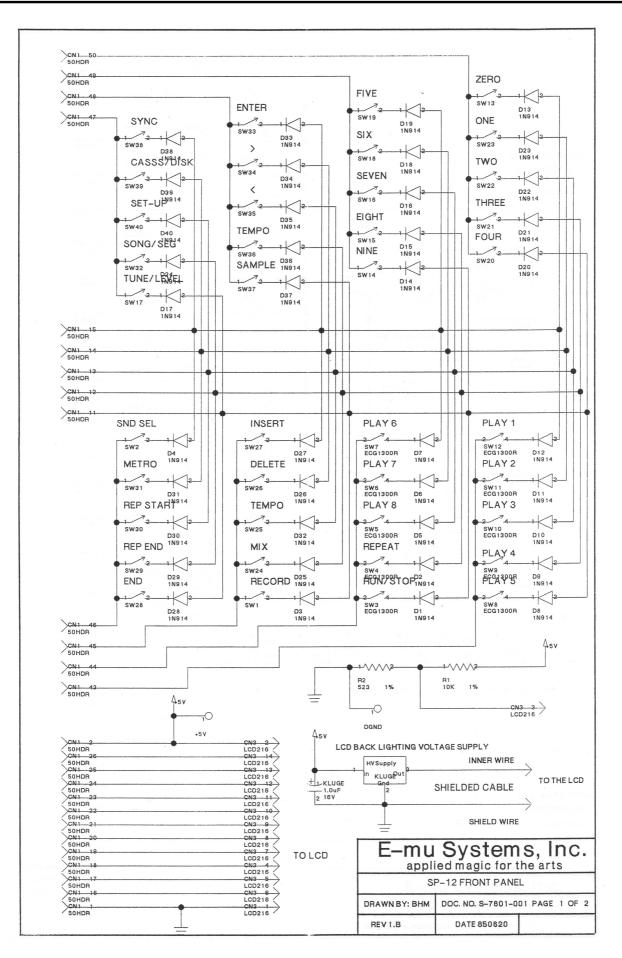
#### SIGNAL NAME DEFINITIONS 59 Name Source Destination Type Description +SDB11.D 10.11 12.13 TTL Snd Data Bus Bit 11 -SELDSK.D 2 TTL SMPTE/Disk Select 4 2 -SELECT CN7 TTL Floppy Select +SHSTB.D 4 15 TTL Sample/Hold Strobe 2 -SIDE CN7 TTL Floppy Disk Side Sel. 2 +SIOIEO.D 2 TTL SIO Int. Ena. Out +SMA0.D 9 10 Snd Mem Addr 0 TTL +SMA1.D 9 10 TTL Snd Mem Addr 1 +SMA2.D 9 10 Snd Mem Addr 2 TTL 9 +SMA3.D 10 TTL Snd Mem Addr 3 9 +SMA4.D 10 TTL Snd Mem Addr 4 +SMA5.D 9 Snd Mem Addr 5 10 TTL 9 +SMA6.D 10 TTL Snd Mem Addr 6 +SMA7.D 9 10 TTL Snd Mem Addr 7 +SMA8.D 9 10 TTL Snd Mem Addr 8 +SMA9.D 9 10 TTL Snd Mem Addr 9 +SMA10.D 9 10 TTL Snd Mem Addr 10 9 +SMA11.D 10 TTL Snd Mem Addr 11 +SMA12.D 9 10 TTL Snd Mem Addr 12 +SMA13.D 9 10 TTL Snd Mem Addr 13 9 +SMA14.D 10 TTL Snd Mem Addr 14 +SMA15.D 9 10 TTL Snd Mem Addr 15 +SMA16.D 8 10 TTL Snd Mem Addr 16 +SMA17.D 8 10 TTL Snd Mem Addr 17 +SMA18.D 8 10 TTL Snd Mem Addr 18 -SMACAS.D 10 11 TTL Snd Mem Addr CAS -SMOE.D 13 10,11 TTL Snd Mem Output En. +SMPAMP.V 8 14 Ana. Volt. Sample Pre-amp Out 2 +SMPRLC.D 4 TTL SMPTE Rec Latch Clk 2 +SMPROS.D 4 SMPTE 1-shot Lch Clk TTL 2 +SMPRXC.D 4 SMPTE Receive Clock TTL 2 -SMPTXC.D 4 TTL SMPTE Transmit Clock 2 -STEP CN7 TTL Floppy Disk Head Step -SWEH.D 13 10,11 Snd Mem Wr Ena Hi TTL -SWEL.D 13 10.11 TTL Snd Mem Wr Ena Lo -TK00 CN7 2 TTL Floppy Track 00 -TOE.D 7 8 Temp Latch Out Ena TTL 2 -TXC.D 4 TTL Transmit Clock +TXD.D 2 4 TTL Transmit Data 7 +UCK.D 8.9 TTL μC Main Clock + -UCK.D 1 4,7,10,13 TTL µC Main Clock -+UCNL0.D 1 7,8,13 TTL uC Chan Addr 0 +UCNL1.D 1 7,8,13 TTL μC Chan Addr 1 +UCNL2.D 1 7,8,13 TTL μC Chan Addr 2

Name	Source	Destination	Туре	Description
+UCNT0. +UCNT1. +UCNT2. -WAIT.D -WD -WP -WR.D -WTGT	D 1	4,7,10,13 4,5,7,10,13,14 4,7,10,13 1 CN7 2 3,4,13 CN7		μC State Counter Bit 0 μC State Counter Bit 1 μC State Counter Bit 2 Z-80 Wait Floppy Disk Write Floppy Write Protect Z-80 Write Floppy Write Gate

# SCHEMATICS

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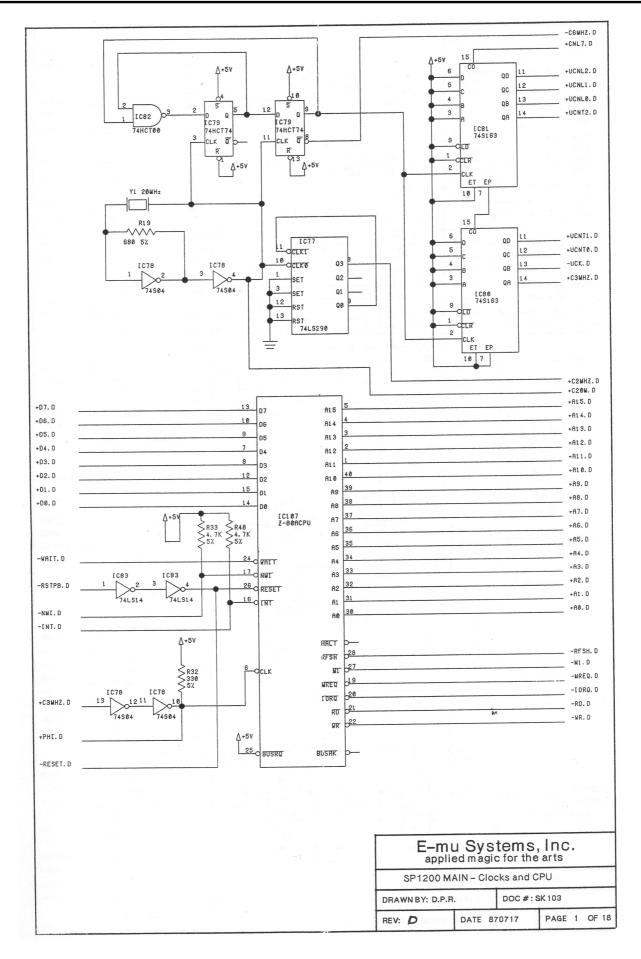




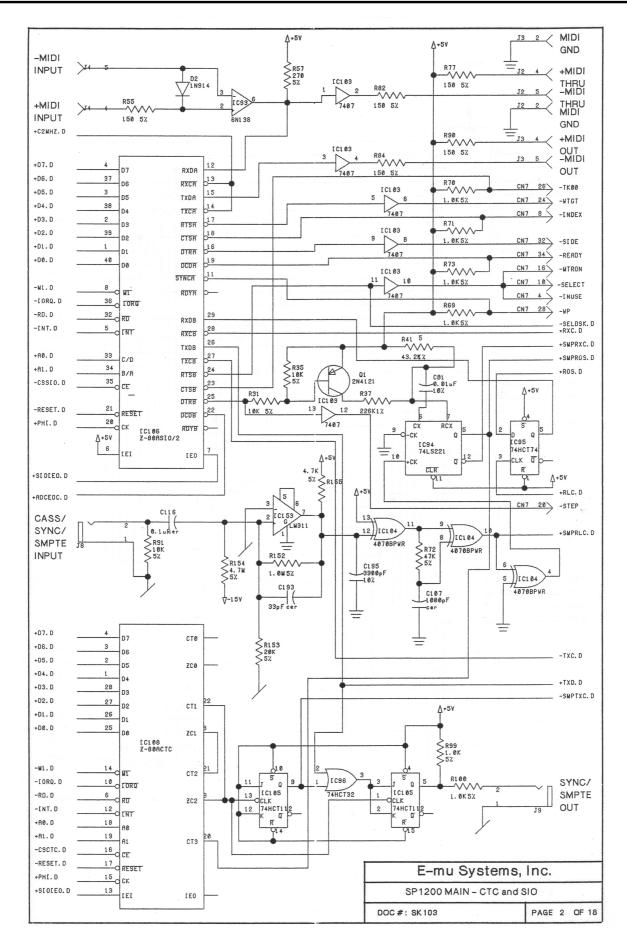
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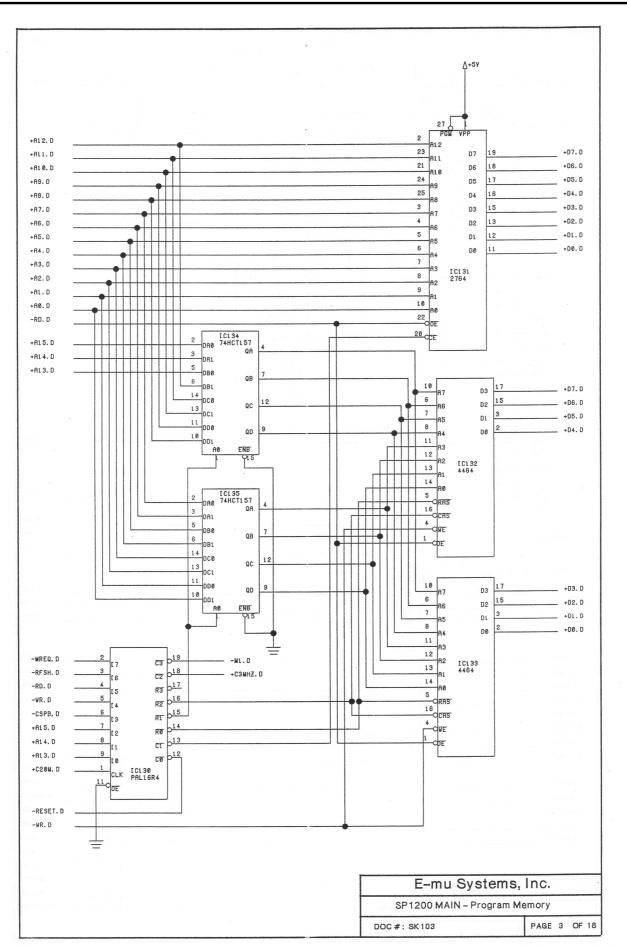
	SET-UP	AA		Å5v					
CN1_42	021-05	-1()2-							
00100	CASS/DISK	LP16 TIL220	29						
CN1 41	CA22/DISK	LED	-1(R)2-						
SOHDR	OVING	RR	LP15 TIL220						
CN1_40	SYNC	-1An-	LED						
50HDR		LP14 TIL220	010					VIOW	RE FROM
CN1 39	SAMPLE	LP14 IIL220 LED	122						YBACK
50HDR				Ť				<i></i>	PSELECT.D
CN138			LP13 TIL220 LED					57	
50HDR	1.5				CAMPLE		1		
CN137	SONG				SAMPLE				
50HDR			-1692-					CN2 4 Molex6	$\geq$
×	SEGMENT	AS-	LP11 TIL220 LED	rise i se	3 GW	KLUGE	KLUGE		
SOHDR		-1(K)2-				+) CT316		CN2 5	$\geq$
	TUNING	LP10 TIL220 LED	AL		10K 2 Log 1	10uF TANT	10uF TANT	Molexo	
CN1 35 50HDR			-1(K)2-		•		<u> </u>		$\geq$
	LEVEL	AL	LP9 TIL220 LED		ME		OL	Molex6 1	
CN1_34 50HDR		-1(()2-	LED						
	DECAY	LP8 TIL220	AA				an a	CN2 2 Molex6	$\geq$
CN1_33 50HDR	DEOM	LED	-1(()2-	•	BI	3 cw			
	SND SEL A	AA	LP7 TIL220		a Same and a second sec				
CN1_32 50HDR	SIND SEL A	-1(2)2-	LED		La	1	1		
50HDR		LP6 TIL220	RR						
CN1_31	SND SEL B	LED	-1				2 5%		
50HDR		00	LP3 TIL220						
CN1 30	SND SEL C	122	LP3 IIL220 LED					CN2 3 Molex6	$\geq$
50HDR			44	1.03	MIX VOL				
CN1 29	SND SEL D	LP2 TIL220 LED				3	çw		
50HDR			- U			HI9 <	> [ ×		
CN1_28	RUN/STOP	AS.	LP1 TIL220 LED			45V 10K Log	2		
50HDR		- KJ2-					1		
×	RECORD	LP5 TIL220 LED		~				CN2 6	$\geq$
CN1_27 50HDR	-1(K)2-							Molex6	
	LP4 TIL220	IDERS 1		-				7	
	5L	C	2	3	4	5	6	7	8
			CW 1 BT7		CW 1		/ /		
			2 10K Linear	2 < 10K Linear	2 10K Linear	2 10K 2 Linear	Linear 2	Linear	2 10K Linear
		3	3	3	3	3 3	3		3
CN1_3	121		•				•	•	
50HDR									
SOHDR			1	4					
CN1 5									
CN1_6									
50HDR				*					
50HDR									MIDEED
CN1_8 50HDR									WIRE FR GYBACK
SOHDR									+ADCIN7.D
CN1 10									0
50HDR									
	'								an an air a sa an
DRG WIRE FROM PIGGYBACK						E-mu	Syster	ns, Ir	nc.
IGG I BAUK							ONT PANEL		

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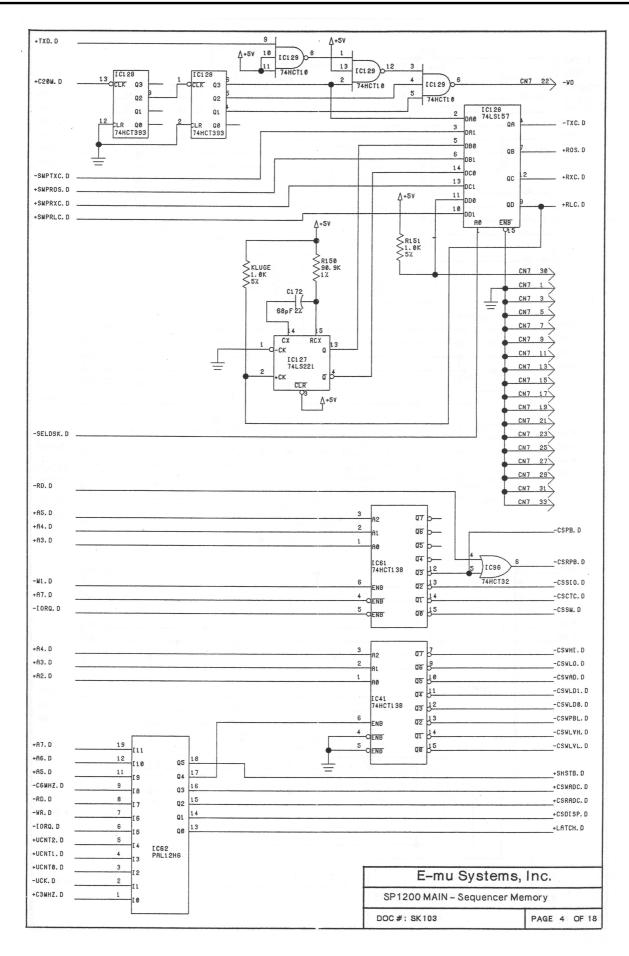


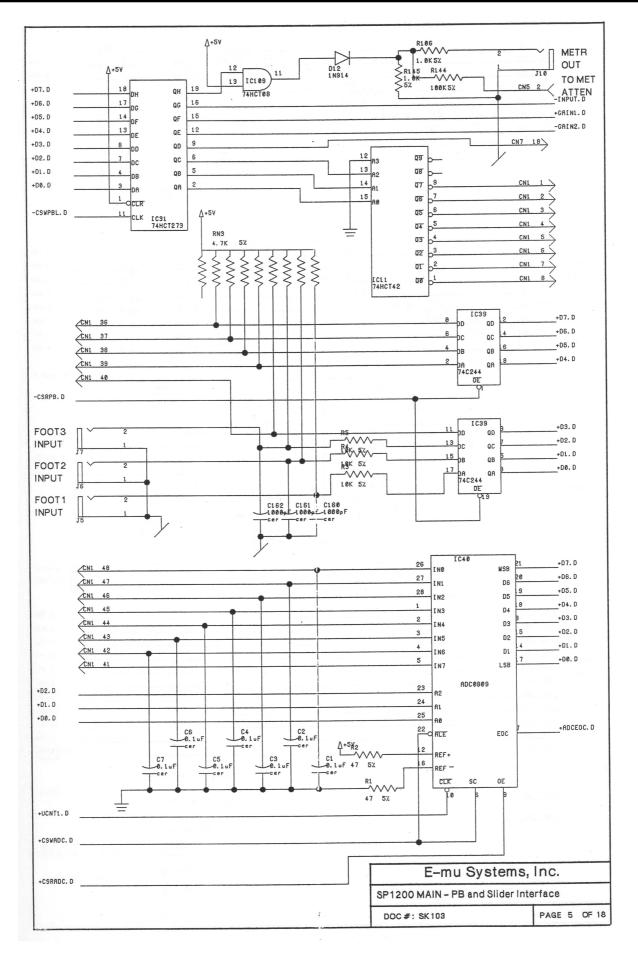
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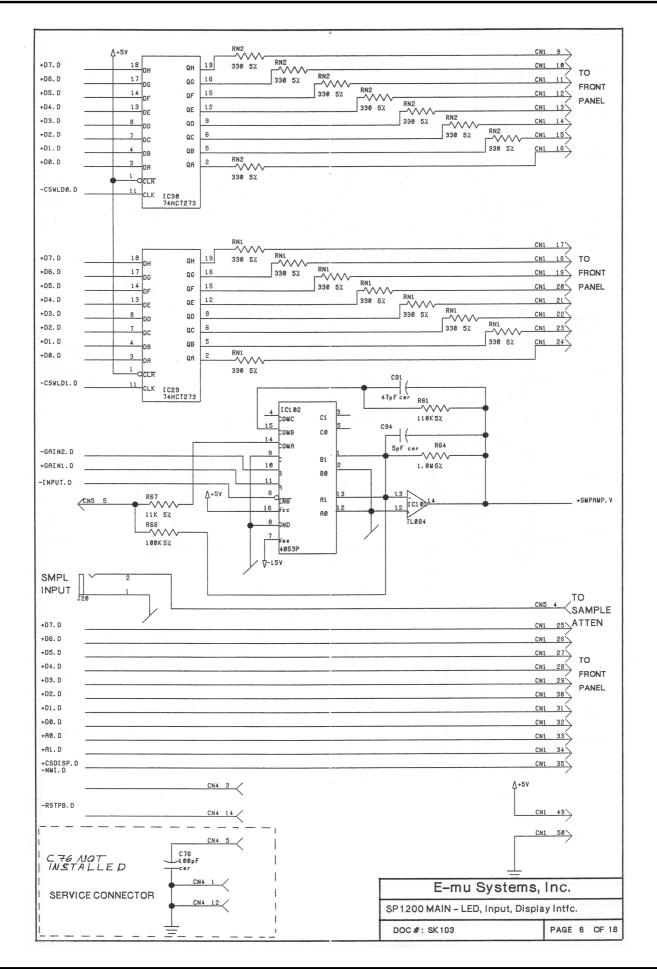




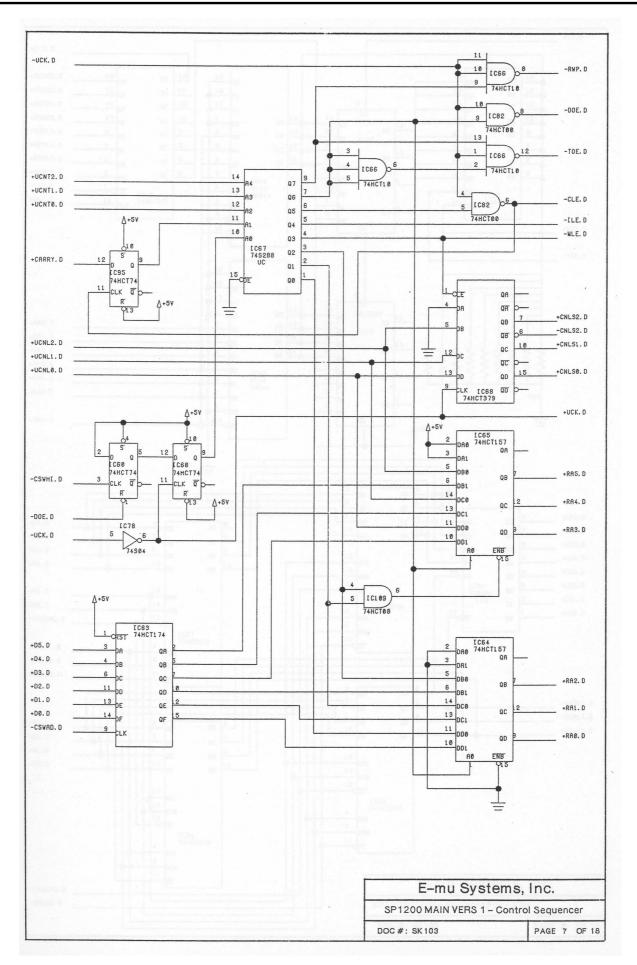
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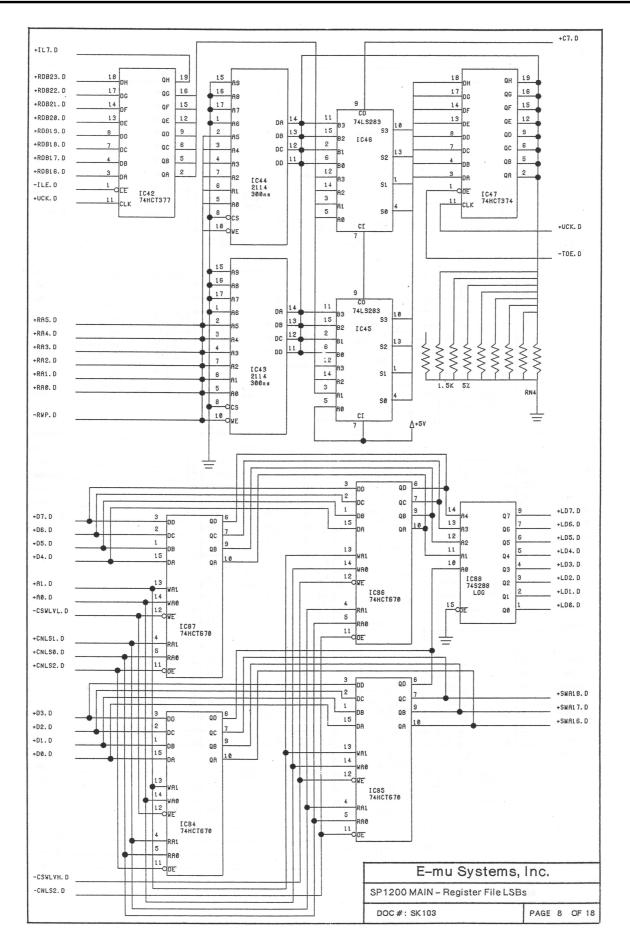


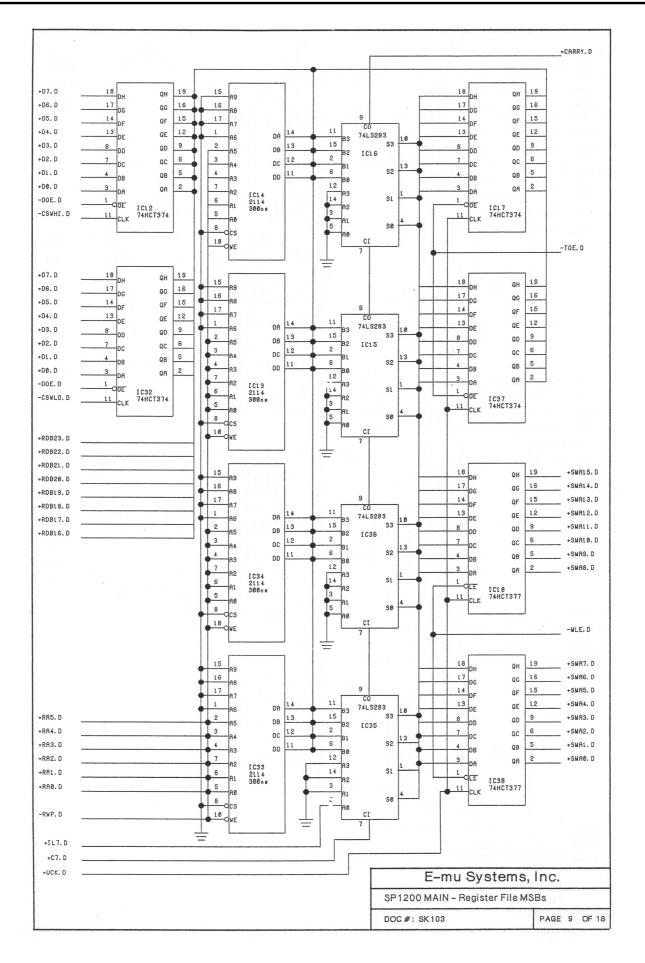


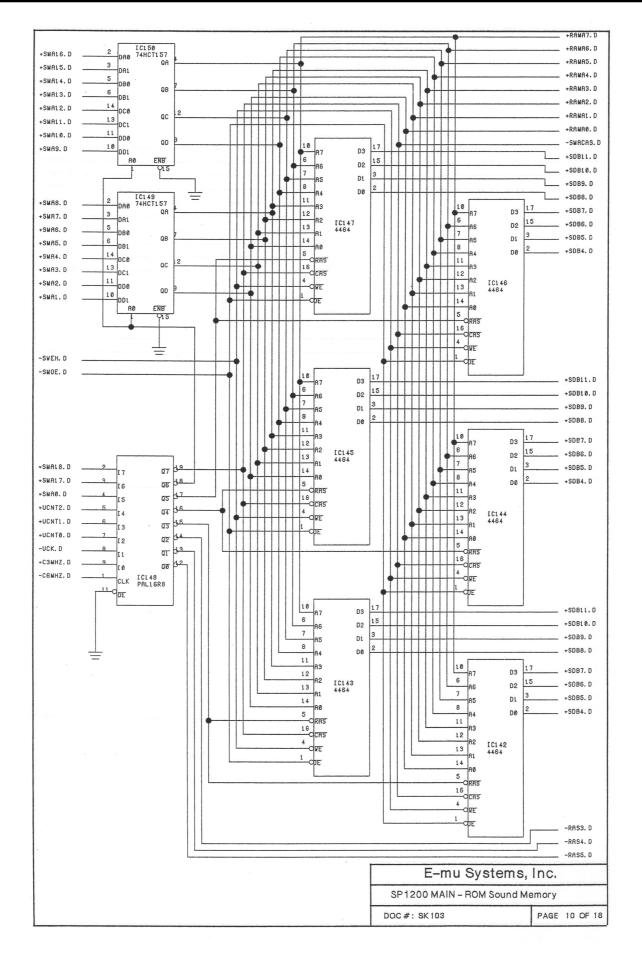


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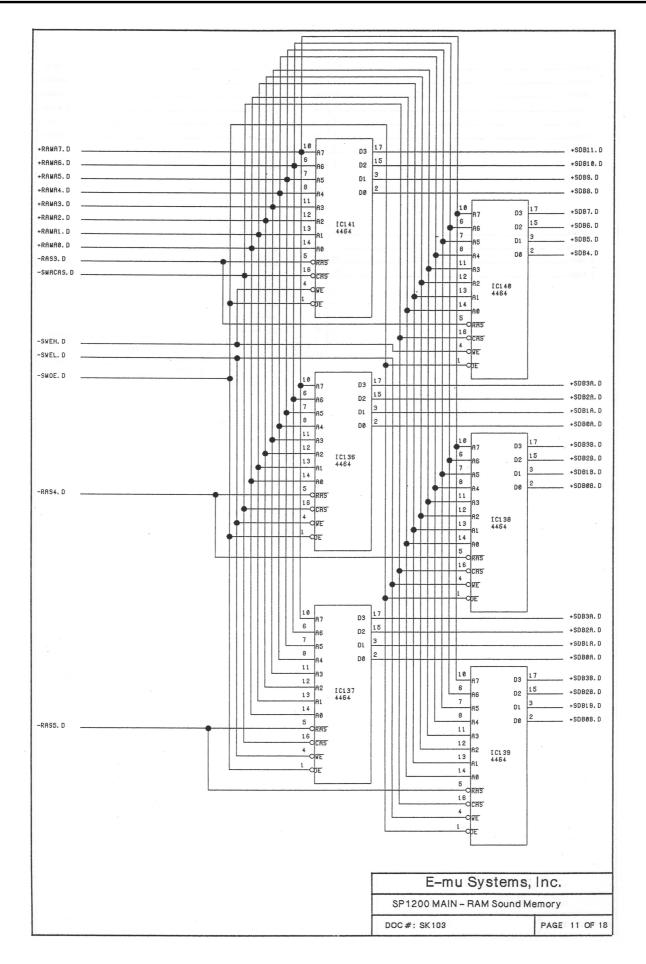






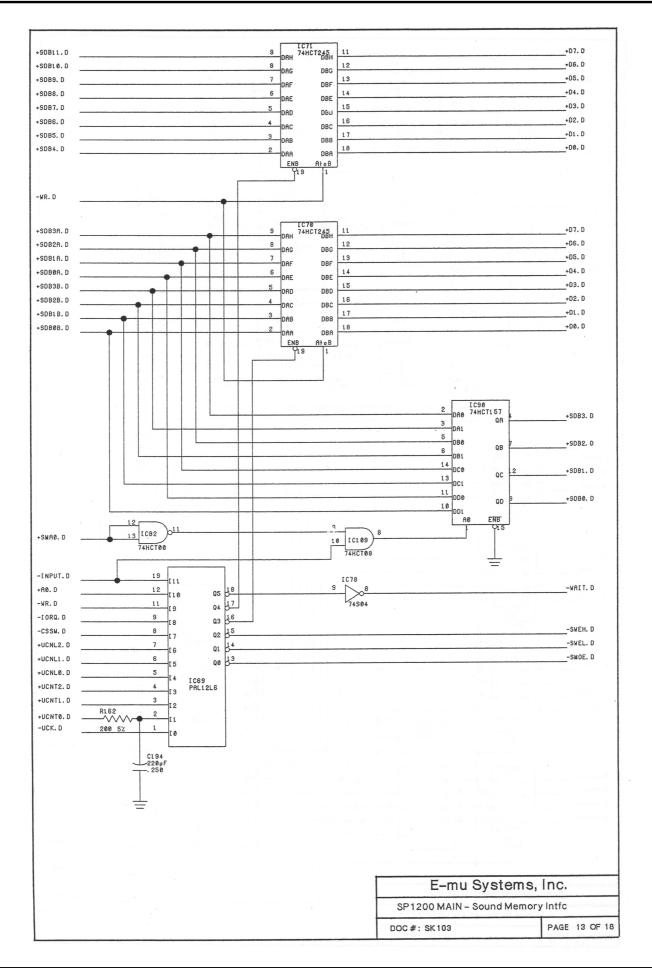


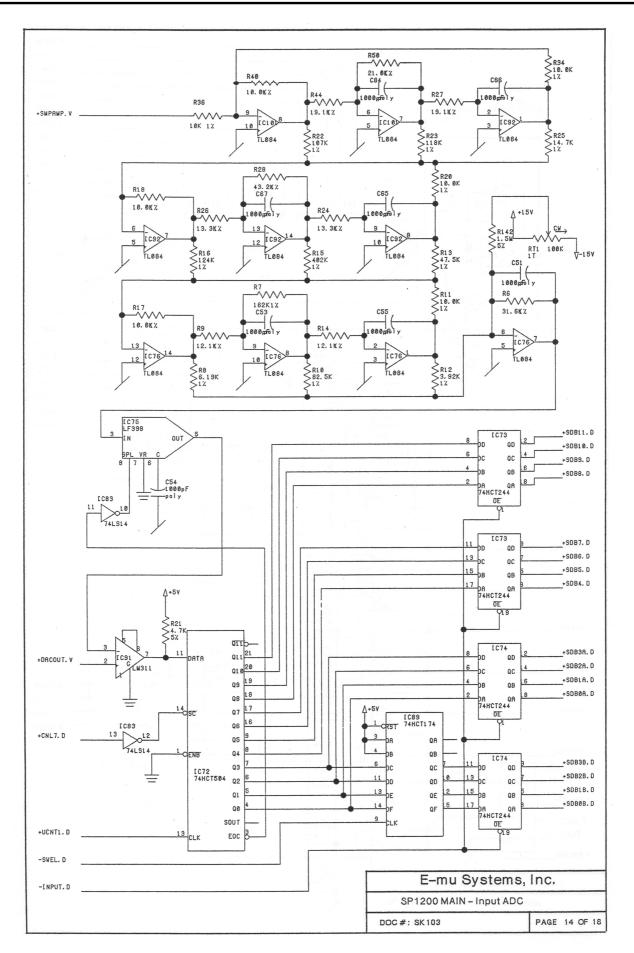
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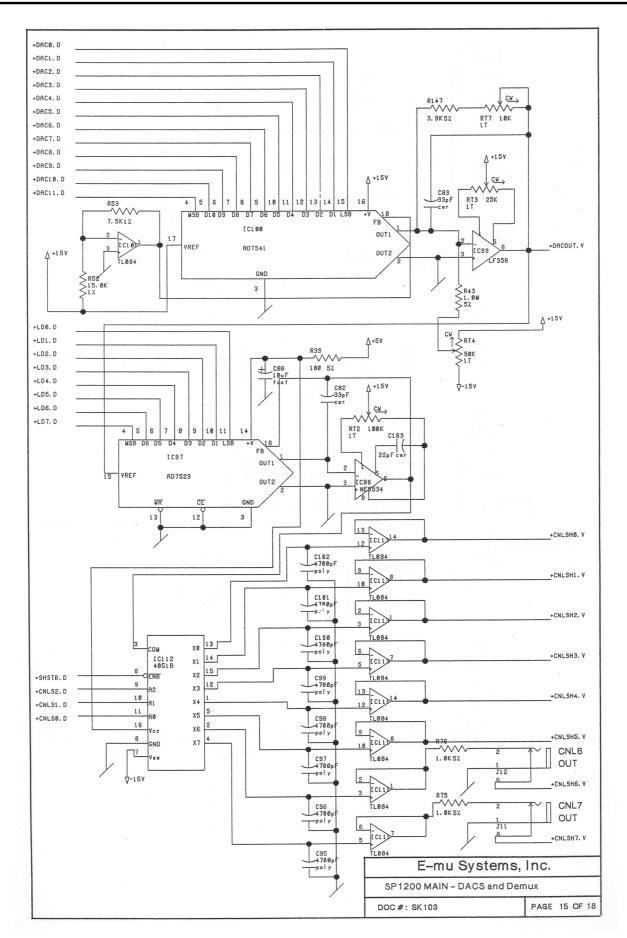
.1.0		18 07 0	17 19		+DAC11.D
0.D		17 06 0	15		+DAC10, D
9. D		14	15		+DAC9. D
3. D		04	14 <u>12</u> 13 9		+DAC8. D
7. D		-			+DAC7. D
5. D		02	12 <u>5</u>		+DAC5. D
4. D		DI	2		+DRC4. D
		1 OE IC151 11 LE 74HCT3			
3. D		18	19		+DAC3. D
2. D		17	16		+DAC2, D
		00	15		+DAC1. D
. D			12		+DAC0. D
		03	23 22 21		
сн. р		3_00	20		
UT.D	5 6 10 IC96 8 74LS14 74HCT32	0E IC152 11 LE 74HCT3	73		
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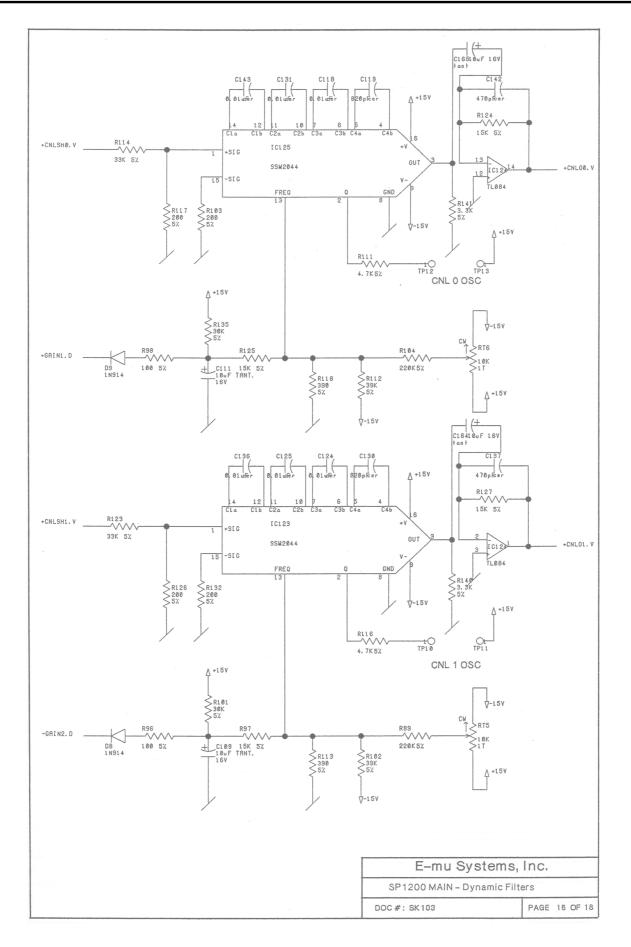


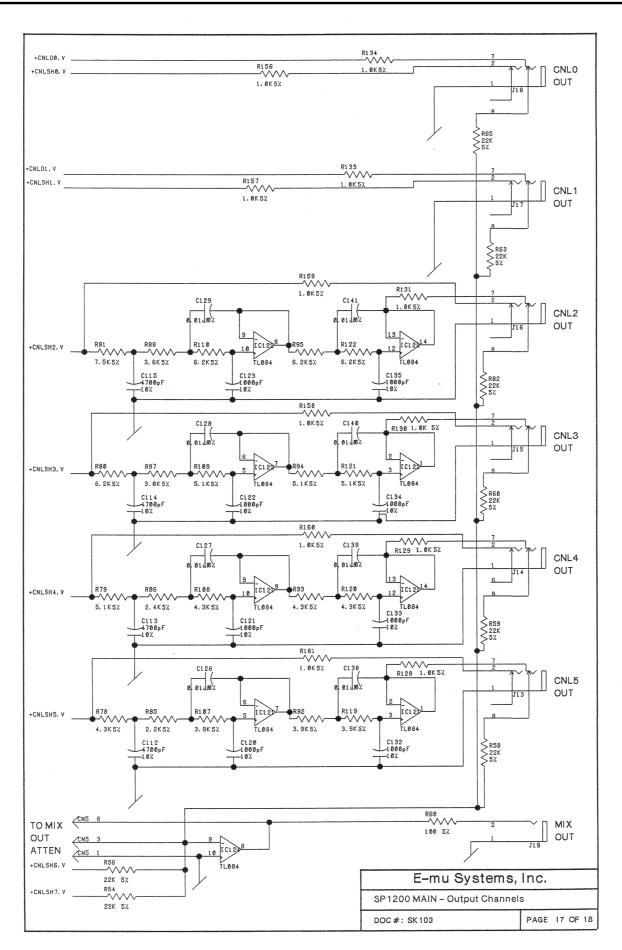


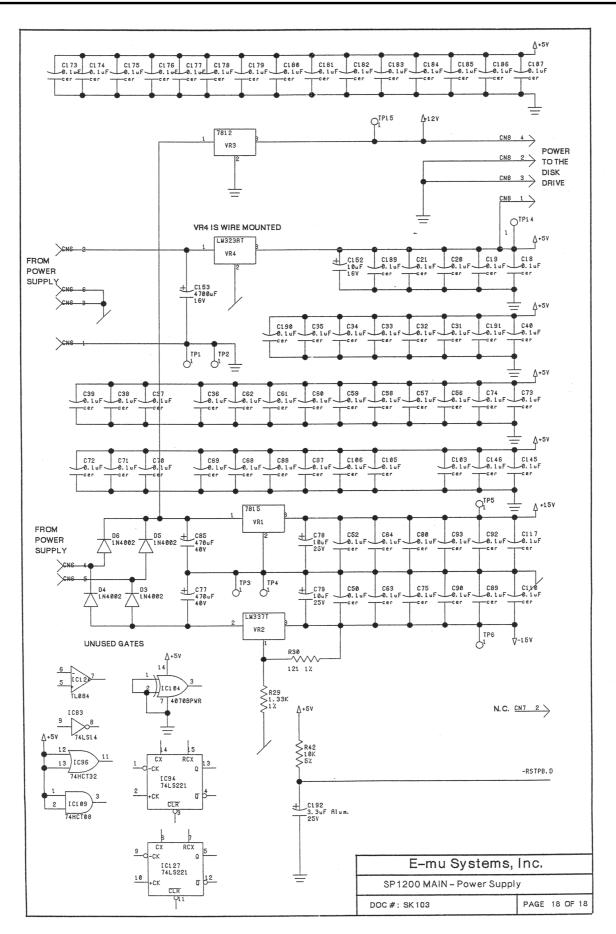




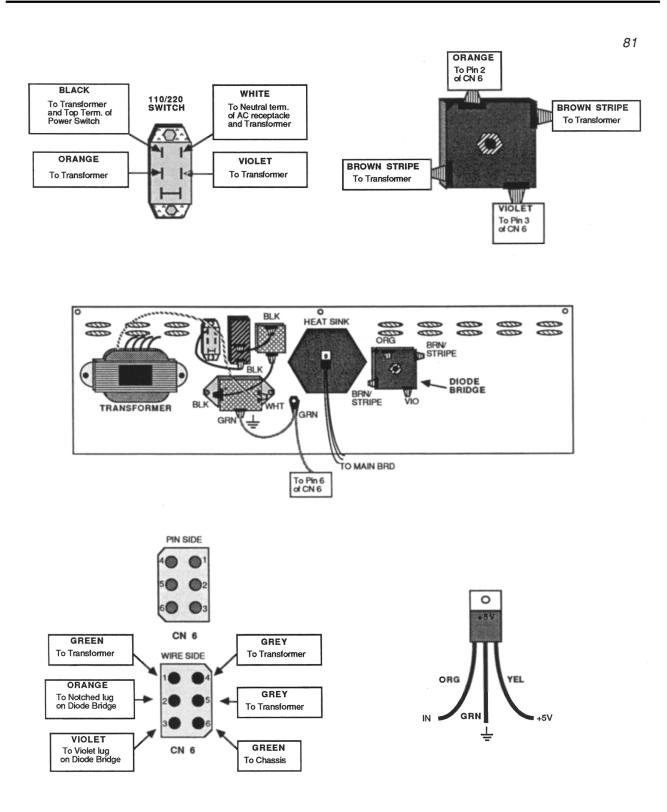




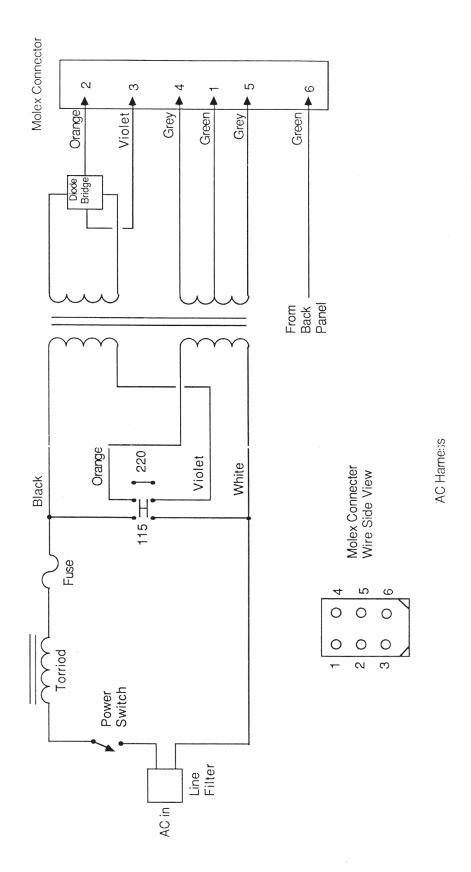


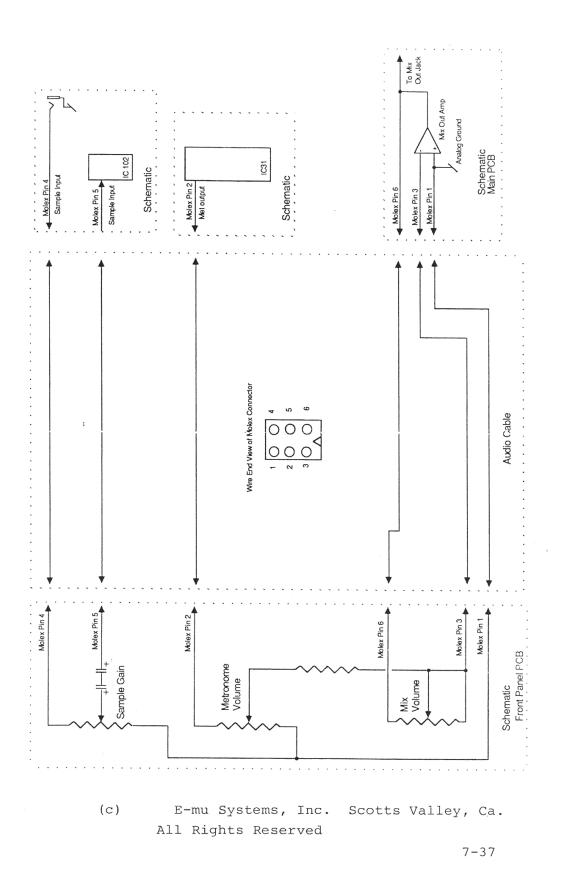


# WIRING DIAGRAMS



SP1200 CHASSIS WIRING





#### SP 1200 PARTS LIST

**ORDERING PARTS:** Parts can be ordered by written order or by phone. When ordering parts, you MUST order by E-mu part number. The minimum parts order is \$15.00. Emergency rush orders can usually be sent out the same day if the order is received by 11:00 PST. Parts orders can be placed between the hours of 8:30 am and 5:30 pm PST Monday through Friday. E-mu Customer Service Department (408) 438-1921.

#### MAIN BOARD

CAPACITORS	E-MU P/N	QUANTITY
470 μF 40V	CA 318	2
4700 μF 16V	CA 319	1
3.3 μF 25V	CA 324	1
220 pF	CC 104	1
22 pF 50V	CC 302	1
470 pF 50V	CC 305	2
820 pF_50V	CC 307	2
4700 pF 50V	CC 309	4
$.01  \mu F 50V$	CC 311	9
$.01  \mu F 50V$	CC 312	6
$.1 \mu\text{F}$ 50V	CC 314	73
1000 pF 100V	CC 324	12
3900 pF 50V	CC 325	1
47 pF 50V	CC 326	1
5 pF 50V	CC 328	
33 pF 50V	CC 329	3
	CM 117	
1000 pF Plas.	CP 107	0
4700 pr Plas.	CP 108	0
$10 \ \mu F$ Tant. $10 \ v$	C1 310	0
470 $\mu$ F 40V 4700 $\mu$ F 16V 3.3 $\mu$ F 25V 220 pF 22 pF 50V 470 pF 50V 820 pF 50V 4700 pF 50V .01 $\mu$ F 50V .01 $\mu$ F 50V .01 $\mu$ F 50V .1 $\mu$ F 50V 1000 pF 100V 3900 pF 50V 47 pF 50V 5 pF 50V 33 pF 50V 5 pF 50V 33 pF 50V 68 pF 1000 pF Plas. 4700 pF Plas. 10 $\mu$ F Tant. 16V 10 $\mu$ F Tant. 25V	CI 317	2
COMPONANT	E-MU P/N	QUANTITY
1/4" Audio Jack Mono	JA 301	8
1/4" 1 CLSD CKT Jack	JA 307	2
1/4" 2 CLSD CKT Jack	JA 310	6
1/4" 2 CLSD CKT Jack 18 pin DIP Socket	JC 105	21

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20 pin DIP Socket 24 pin DIP Socket 28 pin DIP Socket 40 pin DIP Socket 16 pin DIP Socket 5 Pin DIN Socket 6 pin Molex Pwr. Conn AMP Pwr Conn. .100 x4 Male Pwr Conn Rib Header Conn 50 Pin Header	JC 308 JC 309 JC 311 JI 302	8 1 3 2 15 3 2 1 1 1 1 1	
ICs	E-MU P/N	QUANTITY	
Analog and Hybrid ICs 4051 Analog Mux 4053 Analog Switch NE5534 Audio Driver +12V Reg. 1A LF356 BI-FET TL084 Quad Op-Amp SSM 2044 VCF +15V Reg. 1A Adj. Reg. 1.5A 5V Reg. 3A 6N138 Opto-isolator	IL 110 IL 301 IL 302 IL 303 IL 308 IL 321 IL 333	$ \begin{array}{c} 1\\ 1\\ 1\\ 1\\ 8\\ 2\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1 \end{array} $	
Interface ICs LM311 Comparator 7523 MDAC ADC 0809 7541 12 Bit MDAC LF 398 S/H	II 102 II 304 II 336 II 337 II 338	2 1 1 1 1	
$\begin{array}{c} \textbf{Memory ICs and PALs}\\ 2114 SRAM 4K 300 nS\\ 4464 64K x 4 RAM\\ 74S288 \mu C PROM\\ 74S288 Log PROM\\ 74S288 Log PROM\\ Z-80 RAM PAL\\ Chip Select PAL\\ Sound Mem. PAL\\ DRAM PAL\\ 2764 Mainboot EPROM\\ \end{array}$	IM 357 IM 373 IP 326 IP 327 IP 357 IP 358 IP 359 IP 360 IP 362	6 14 1 1 1 1 1 1 1	

		PA	RTS LIST	87
				-
Digital ICs	10 101			
4070 Quad XOR	IC 131	1		
74C2 Tri-State Buffer	IC 341	1		
Z-80A CPU	IM 343	1		
Z-80A SIO/2	IM 344	1		
Z-80A Counter/Timer	IM 346	1		
7407 Hex Buffer	IT 104	1		
74LS290 Decade Counter	IT 122	1		
74LS14 Hex Schm. Trig.	IT 307	1		
74LS157 Quad Mux.	IT 313	1		
74LS221 Dual 1-Shot	IT 316	2		
74LS283 Bin Adder	IT 318	6		
74S161 Bin Counter	IT 331	2		
74HCT32 Quad AND	IT 354	1		
74HCT74 Dual D FI-FI	IT 355	3		
74HCT138 3-8 Decoder	IT 357	2		
74HCT174 Hex D F-F	IT 359	2		
74HCT244 Oct Buffer	IT 360	2		
74HCT273 Oct Fl-Fl	IT 361	2		
74HCT374 Oct Fl-Fl	IT 362	2 2 2 3 5		
74HCT08 Quad AND	IT 363	1		
74HCT393 4-Bit Dual	IT 364	1		
74HCT42 BCD>Dec	IT 366	1		
74HCT12 DCD-22Dec 74HCT10 Tri NAND	IT 368	2		
74HCT00 Quad NAND	IT 369	1		
74HCT670 4x4 Reg File	IT 371	4		
74S04 Hex Inv.	IT 375	1		
74LS379 Quad Fl-Fl	IT 377	1		
74HCT157 Quad Mux	IT 379	7		
74HCT504	IT 381	1		
74HCT245 Oct Buffer	IT 383	2		
74HCT377 Oct D Fl-Fl	IT 384	3		
74HCT112 J-K Fl-Fl	IT 385	1		
74HCT373 Oct Latch	IT 391	2		
74IICI575 Oct Latell	11 391	2		
RESISTORS	E-MU P/N	QUANTITY		
		_,		
4.7K $\Omega \ge 9$ Res. Net. SIP	RN 319	1		
330 $\Omega$ x8 Res. Net.	RN 320	2		
1.5KΩ x9 Res. Net. 10 pin		1		
	RP 106	7		
	RP 107	1		
-	RP 110	1		
	RP 304	ī		
	RP 309	î		
	RP 312	$\hat{2}$		
$121 \Omega 1/4 W 1\%$	RP 315	1		
	10 010	-		

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21K Ω 1/4 W 1%	RP 317	1	
13.3K Ω 1/4 W 1%	RP 318	$\hat{2}$	
19.1K Ω 1/4 W 1%	RP 320	$\frac{1}{2}$	
$1.33K \Omega 1/4 W 1\%$	RP 321	1	
$43.2K \Omega 1/4 W 1\%$	RP 323	$\hat{2}$	
$162K \Omega 1/4 W 1\%$	RP 324	1	
$47.5K \Omega 1/4 W 1\%$	RP 335	1	
31.6K $\Omega$ 1/4 W 1%	RP 337	1	
$402K \Omega 1/4 W 1\%$	RP 342	1 -	
$6.19K \Omega 1/4 W 1\%$	RP 344	1	
$82.5K \Omega 1/4 W 1\%$	RP 345	1	
$3.92K \Omega 1/4 W 1\%$	RP 346	1	
		1	
$107K \Omega 1/4 W 1\%$	RP 347		
118K Ω $1/4$ W 1%	RP 348	1	
14.7K Ω 1/4 W 1%		1	
$7.5K \Omega 1/4 W 1\%$		1	
$150 \Omega 1/4 W$	RR 102	5	
$3.3 \mathrm{K} \Omega 1/4 \mathrm{W}$	RR 110	2	
47K Ω 1/4 W 4.7M Ω 1/4 W 4.7M Ω 1/4 W	RR 122	1	
$4.7M \Omega 1/4 W$	RR 132	1	
4/ <u>1</u> /4 W	RR 133	2	
$100 \Omega 1/4 W$	RR 301	4	
200 Ω 1/4 W	RR 302	5	
330 Ω 1/4 W	RR 303	1	
390 Ω 1/4 W	RR 304	2	
$1K\Omega 1/4 W$	RR 305	24	
$4.7 \mathrm{K} \Omega 1/4 \mathrm{W}$	RR 307	6	
$10K \Omega 1/4 W$	RR 309	7	
$11K \Omega 1/4 W$	RR 310	1	
15K Ω 1/4 W	RR 311	4	
$22K \Omega 1/4 W$	RR 313	8	
$30K \Omega 1/4 W$	RR 315	2	
33K Ω 1/4 W	RR 316	2	
39K Ω 1/4 W	RR 317	2	
100K Ω 1/4 W	RR 318	2	
20K Ω 1/4 W	RR 323	1	
$1M \Omega 1/4 W$	RR 325	3	
3K Ω 1/4 W	RR 327	1	
$1.5M \Omega 1/4 W$	RR 332	1	
220K Ω 1/4 W	RR 335	2	
2.2K Ω 1/4 W	RR 337	1	
110K Ω 1/4 W	RR 342	1	
680 Ω 1/4 W	RR 343	1	
270 Ω 1/4 W	RR 347	1	
7.5K Ω 1/4 W	RR 351	1	
6.2K Ω 1/4 W	RR 352	4	
5.1K Ω 1/4 W	RR 353	4	
4.3K Ω 1/4 W	RR 354	4	
3.9K Ω 1/4 W	RR 355	4	

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			PARTS LIST 89
25K $\Omega$ Trim 50K $\Omega$ Trim	RR 356 RR 357 RT 301 RT 307 RT 308 RT 309	1 1 3 1 1 2	
MISCELLANEOUS	E-MU P/N	QUANT	ITY
1N914 Signal Diode 1N4002 Rect. Diode 2N411 PNP Trans 20 mHz Crystal	DD301 DD 302 QQ 101 ZX 304	4 4 1 1	
	FRONT PA	NEL	
PART NAME	E-MU P/N	QUANT	ТТҮ
Piezo Xtal Assy	AD 341	1	
100 pF Cap. .02 μF 50V Cap. .1 μF 50V Cap. 1 μF Tant 25V Cap. 10 μF Tant 16V Cap.	CC 103 CC 313 CC 314 CT 315 CT 316	1 1 1 3	
1N914 Diode	DD 301	41	
4-40 Kepf Nut 3/8-32 Nut 4-40 x 3/8 Screw 3mm x10mm Ph. Screw Nylon Spacer #4 Nylon Washer 3/8" Lock Washer	HN 304 HN 311 HS 302 HS 325 HS 369 HW 210 HW 312	$     \begin{array}{c}       4 \\       3 \\       4 \\       16 \\       16 \\       4 \\       3     \end{array} $	
14053 Analog Mux TLC27N Quad Op-Amp	IC 345 IL 324	1 1	
6 Pin Molex Pwr Conn. 50 Pin Rib Header	JP 111 JR 301	1 1	
LCD 16 x 2 lines Red LED	LP 304 LP 311	1 15	

RC 302	3
RC 311	8
RP 106	1
RP 308	1
RR 307	1
RR 309	3
RR 311	2
RR 318	1
RR 328	1
RR 338	1
RT 309	1
SW 301	10
SW 306	1
SW 312	28
ZV 300	1
	RT 309 SW 301 SW 306

#### **CHASSIS**

PART NAME	E-MU P/N	QUANTITY
Diode Bridge 5A 50V	DB 300	1
Chassis (Bottom Panel) Reg. Heatsink Plastic Housing 1200	EM 354 EM 359 EP 324	1 1 1
Slider Knob Rotary Knob (No Cap) Rotary Knob Cap	HK 313 HK 314 HK 315	8 3 3
3/8 x 32 Panel Nut 4-40 Kepf Nut 8-32 Kepf Nut 8-32 x 3/8" Ph. Screw 4-40 x 3/8" Standoff 4-40 x 1/4" SEM Screw 6-32 x 1/4" SEM Screw 8-18 x 3/8" Inplas Screw 3/8" Panel Washer	HS 351 HS 352 HS 353	$16 \\ 2 \\ 4 \\ 4 \\ 3 \\ 13 \\ 12 \\ 8 \\ 16$
Fuse Holder Red Fuse Cap AC Pwr Conn/RFI Filt.	JC 124 JC 137 JP 310	1 1 1
Power Switch	SW 103	1

and the second

		PARTS LIST 91
110/220 Switch	SW 107	1
Fuse 2A Slo-blo Front Panel Label 3.5" Floppy Disk Drive Front Pnl Fisch Paper Rubber Foot Power Transformer	ZF 102 ZL 361 ZM 336 ZP 323 ZR 308 ZT 307	1 1 1 4 1
MISCELLANEOUS	E-MU P/N	QUANTITY
Set of 5 Prod. Disks SP1200 Op. Manual Power Cord US Power Cord W. Europe SP1200 Shipping Box Left Shipping Foam Right Shipping Foam	AD 358 FI 332 WC 116 WC 308 ZS 364 ZS 365 ZS 366	1 1 1 or 1 1 1 1
	CABLES	1
PART NAME	E-MU P/N	QUANTITY
Front Panel Audio Cable Interpanel Data Cable Disk Data Cable Disk Power Cable Female Molex Pin Male Molex Pin	AD 335 AD 345 AD 353 AD 354 JP 305 JP 306	1 1 1 -

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# E.C.O.'s

9/87

### E-mu Systems, Inc.

### SP1200 Sampling Percussion System

### SERVICE/WARRANTY CENTER POLICIES

#### WHAT IT'S ALL ABOUT

This service program covers E-mu Systems SP1200 equipment. It is highly recommended that Service/Warranty Centers have adequate supplies of spare parts on hand to efficiently represent E-mu Systems. Service/Warranty Centers should conduct business in a professional manner and provide E-mu with information concerning product quality and customer needs.

#### SP1200 PRODUCT WARRANTY

E-mu Systems warranty covers all defects in materials and workmanship for a period of ONE YEAR (90 days for disk drives) from the date of purchase by the original owner. The warranty does not cover:

1. Damages due to improper or inadequate maintenance, accident, misuse, abuse, alteration, unauthorized repairs, tampering, or failure to follow normal operating procedures as outlined in the user's manual.

2. Damage or deterioration of cabinet or keyboard.

3. Damages occurring during any shipment of the product for any reason.

4. Any product that has been modified in any way by anyone other than E-mu Systems, Inc. or E-mu Authorized Service/Warranty Centers.

#### SERVICE CENTER

E-mu Authorized Service Centers will provide for warranty and nonwarranty repair of *SP1200* equipment. Service Centers will perform required updates, repair PCB's, and exchange failed parts.

#### WARRANTY CENTER

E-mu Authorized Warranty Centers will provide for warranty and nonwarranty repair of *SP1200* equipment. Warranty Centers will exchange failed parts ONLY. Warranty Centers WILL NOT perform component repair on *SP1200* PCB's.

#### WARRANTY PARTS

Warranty parts are those belonging to a warranty *SP1200* System and those parts held as warranty inventory by a Service/Warranty Center. E-mu will replace any faulty warranty parts or components due to defective workmanship or materials.

#### WARRANTY PARTS RETURN

Warranty parts to be returned will require a Return Authorization. Please call E-mu Service Department for authorization and write the number on the outside of the package. Service/Warranty Centers are responsible for all freight charges incurred when returning parts to Emu Systems, Inc.

#### WARRANTY SWAP

Provided the Center has adequate credit terms with E-mu, a replacement part will be billed and sent freight prepaid before the failed part is returned. A Return Authorization will be assigned to the replacement part and should be used when returning the failed part. The Return Authorization should be written on the outside of the return package. Failed parts will be credited to the Service/Warranty Center account provided they are received at E-mu within sixty days (ninety days for International) of initial Warranty Swap. Service/Warranty Centers Domestic and International are responsible for all freight charges incurred when returning parts to E-mu Systems, Inc.

<u>INTERNATIONAL NOTE</u> \* It is recommended that parts are consolidated and shipped bulk freight. Freight collect charges will be refused and parts will not be credited to the account. Any duties incurred importing a replacement part may be reclaimed from local customs service when exporting the failed part.

#### WARRANTY CLAIMS

E-mu will reimburse Service/Warranty Centers for warranty work performed on *SP1200* equipment. In order to be eligible for reimbursement, please submit a completed Warranty Claim Form, a copy of Customer Proof of Purchase, and return within SIXTY days of repair date.

Parts used for warranty repair should be listed on the Warranty Claim Form and returned for replacement. Credit will NOT be issued for parts returned other than WARRANTY SWAP (see above).

#### ECO'S

E-mu will provide Service/Warranty Centers with ECO's recommended to improve the performance of the SP1200.

#### CREDIT TERMS

Credit terms are required to receive Warranty Swaps. Please contact our Accounts Payable Department to inquire.

#### FACTORY AUTHORIZATION

If any questions or problems arise regarding Warranty Repair or Warranty Swap, please call for authorization before working on the *SP1200*.

#### TECHNICAL SUPPORT

E-mu Systems provides Service/Warranty Centers with telephone support lines to assistance in resolving technical questions. Telephone support hours are between 8:30am and 5:30pm PST Monday through Friday. E-mu Service Department (408) 438-1921.

#### FACTORY REPAIRS

If the Service/Warranty Center is unable to resolve the failure, please notify E-mu Service and request a Return Authorization.

# **SP1200 CREDITS**

## SP1200 Credits

### HARDWARE DESIGN Dave Rossum SOFTWARE DESIGN **Bill Aspromonte** Tony Dean Marc Ferguson Dave Rossum FUNCTIONAL DESIGN Marco Alpert Marc Ferguson Dave Rossum MECHANICAL DESIGN Ken Provost INDUSTRIAL DESIGN Max Yoshimoto PROJECT MANAGEMENT Tony Dean SOUND PROCESSING Dan Borba Kevin Monahan **TECH MANUAL** Steve Davies (SP-12) Riley Smith (SP1200, diagrams) Nancy Enge (Cover) SPECIAL THANKS Dave Rossum Roger Sheehan E-mu Service Dept.